MAIN FEATURES

- 8-bit resolution.
- ADC gain adjust.
- 2 GHz full power input bandwidth.
- 1 Gsps (min) sampling rate.
- SINAD = 45 dB (7.4 Effective Bits) SFDR = 58 dBc
  @ F_S = 1 Gsps, F_{IN} = 20 MHz :
- SINAD = 44 dB (7.2 Effective Bits) SFDR = 56 dBc
  @ F_S = 1 Gsps, F_{IN} = 500 MHz :
- SINAD = 42 dB (7.0 Effective Bits) SFDR = 52 dBc
  @ F_S = 1 Gsps, F_{IN} = 1000 MHz (-3 dB FS)
- 2-tone IMD : -52dBc (489 MHz, 490 MHz) @ 1GSPS.
- DNL = 0.4 LSB INL = 0.7 LSB.
- Low Bit Error Rate (10^{-13}) @ 1 Gsps
- Very low input capacitance : 0.4 pF
- 500 mVpp differential or single-ended analog inputs.
- Differential or single-ended 50Ω ECL compatible clock inputs.
- ECL or LVDS/HSTL output compatibility.
- Data ready output with asynchronous reset.
- Gray or Binary selectable output data ; NRZ output mode.
- Power consumption : 3.6 W @ Tj = 70°C
  3.8 W @ Tj =125°C
- Dual power supply : ± 5 V
- Radiation tolerance oriented design (150 Krad (Si) measured).

APPLICATIONS

- Digital Sampling Oscilloscopes.
- Satellite receiver.
- Electronic countermeasures / Electronic warfare.
- Direct RF down – conversion.

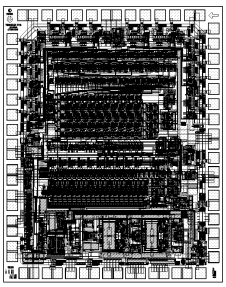
SCREENING

- Atmel-Grenoble standard die flow.
- Mil-PRF-38535, QML level Q for package version.
- Space screening according to ESA/SCC 9000.
- Temperature range : -55°C < Tc ; Tj < +125°C

DESCRIPTION

The JTS8388B is a monolithic 8–bit analog–to–digital converter, designed for digitizing wide bandwidth analog signals at very high sampling rates of up to 1 Gsps.

The JTS8388B is using an innovative architecture, including an on chip Sample and Hold (S/H), and is fabricated with an advanced high speed bipolar process (B6HF from Siemens).
The on–chip S/H has a 2 GHz full power input bandwidth, providing excellent dynamic performance in undersampling applications (High IF digitizing).



ADC 8-bit 1 Gsps

JTS8388B

1/ Delivered in die form

2/ Chip Evaluation Board : Available TSEV8388B

3/ CQFP68 packaged device available : refer to TS8388BF datasheet

4/ Other possible packaging : contact sales office

Novembre 2000

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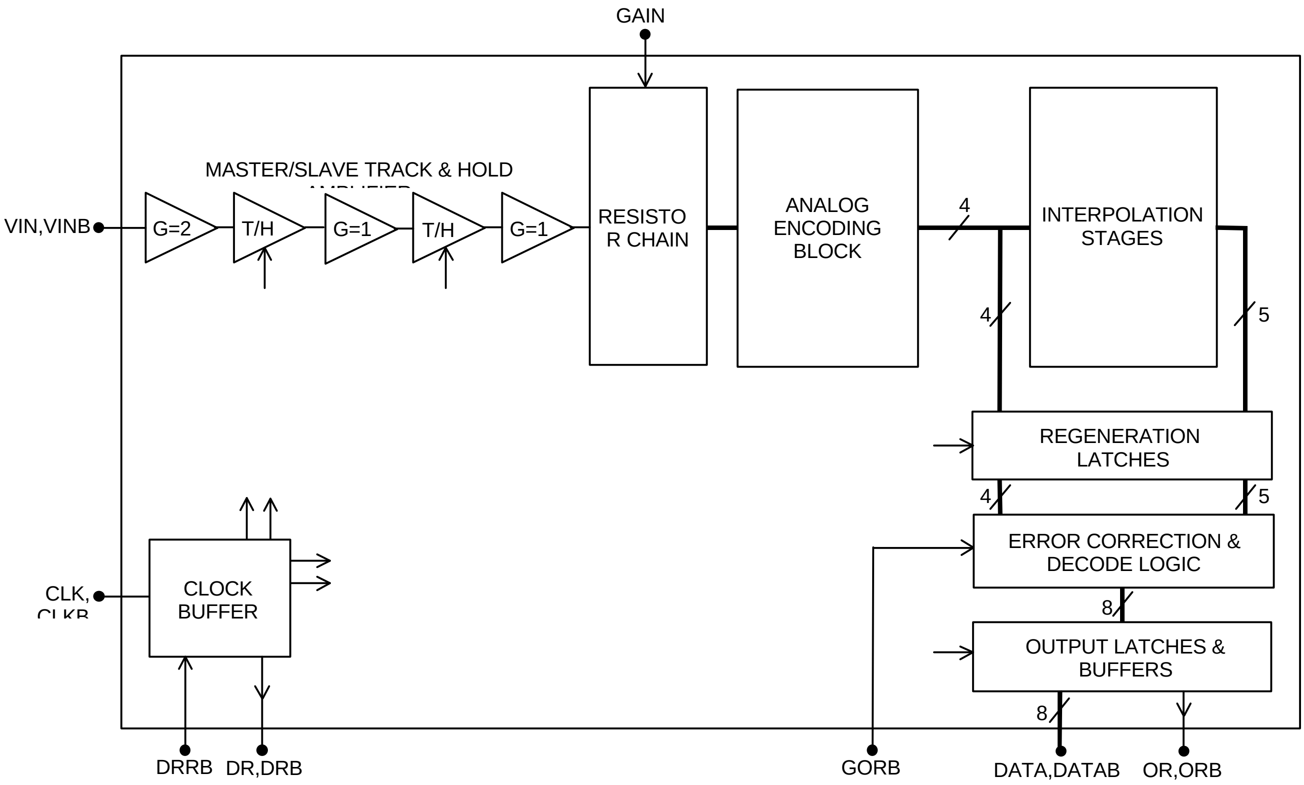
1. SIMPLIFIED BLOCK DIAGRAM



2. FUNCTIONAL DESCRIPTION

The JTS8388B is an 8 bit 1Gsps ADC based on an advanced high speed bipolar technology (B6HF from SIEMENS) featuring a cutoff frequency of 25 GHz.

The JTS8388B includes a front-end master/slave Track and Hold stage (S/H), followed by an analog encoding stage and interpolation circuitry.

Successive banks of latches are regenerating the analog residues into logical data before entering an error correction circuitry and a resynchronization stage followed by 75 Ω differential output buffers.

The JTS8388B works in fully differential mode from analog inputs up to digital outputs.

The JTS8388B features a full power input bandwidth of 2 GHz.

Control pin GORB is provided to select either Gray or Binary data output format.

Gain control pin is provided in order to adjust the ADC gain.

The JTS8388B uses only vertical isolated NPN transistors together with oxide isolated polysilicon resistors, providing enhanced radiation tolerance (no performance drift measured at 150kRad total dose).

3. SPECIFICATIONS

3.1. ABSOLUTE MAXIMUM RATINGS (SEE NOTES BELOW)

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Digital negative supply voltage	DV_{EE}		GND to -5.7	V
Digital positive supply voltage	V_{PLUSD}		GND-0.3 to 2.8	V
Negative supply voltage	V_{EE}		GND to -6	V
Maximum difference between negative supply voltages	DV_{EE} to V_{EE}		0.3	V
Analog input voltages	V_{IN} or V_{INB}		-1 to +1	V
Maximum difference between V_{IN} and V_{INB}	$V_{IN} - V_{INB}$		-2 to +2	V
Digital input voltage	V_D	GORB	-0.3 to V_{CC} +0.3	V
Digital input voltage	V_D	DRRB	V_{EE} -0.3 to +0.9	V
Digital output voltage	Vo		V_{PLUSD}-3 to V_{PLUSD} -0.5	V
Clock input voltage	V_{CLK} or V_{CLKB}		-3 to +1.5	V
Maximum difference between V_{CLK} and V_{CLKB}	$V_{CLK} - V_{CLKB}$		-2 to +2	V
Maximum junction temperature	T_j		+135	^oC
Storage temperature	T_{stg}		-65 to +150	^oC
Lead temperature (soldering 10s)	T_{leads}		+300	^oC

Notes : Absolute maximum ratings are limiting values (referenced to GND=0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum rating may affect device reliability.
The use of a thermal heat sink is mandatory (see Thermal characteristics page 19).

3.2. RECOMMENDED CONDITIONS OF USE

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Positive supply voltage	V_{CC}		4.75	+5	5.25	V
Positive digital supply voltage	V_{PLUSD}	ECL output compatibility		GND		V
	V_{PLUSD}	LVDS output compatibility	+1.4	+2.4	+2.6	V
Negative supply voltages	$V_{EE,\ DVEE}$		-5.25	-5.0	-4.75	V
Differential analog input voltage (Full Scale)	V_{IN}, V_{INB} V_{IN} -V_{INB}	50 Ω differential or single-ended	±113 450	±125 500	±137 550	mV mVpp
Clock input power level	P_{CLK} P_{CLKB}	50 Ω single–ended clock input	3	4	10	dBm
Operating temperature range	T_J	Civil : “C” grade Industrial : “V” grade Military : “M” grade	0 < Tc < 70 -40 < Tc < 85 -55 < Tc ; Tj < +125			^oC

3.3. ELECTRICAL OPERATING CHARACTERISTICS

VEE = DVEE = -5 V ; V_{CC} = +5 V ; V_{IN} -V_{INB} = 500 mVpp Full Scale differential input ;
Digital outputs 75 or 50 Ω differentially terminated ;
Tj (typical) = 70°C. Full temperature range : up to -55°C < Tc ; Tj < +125°C

Parameter		Symb	Temp	Test level	Min	Typ	Max	Unit
POWER REQUIREMENTS								
Positive supply voltage	Analog	VCC		II,IV	4.75	5	5.25	V
	Digital (ECL)	V_{PLUSD}				0		V
	Digital (LVDS)	V_{PLUSD}			1.4	2.4	2.6	V
Positive supply current	Analog	ICC		II, IV		400	425	mA
	Digital	I_{PLUSD}				120	130	mA
Negative supply voltage		VEE	Full	IV	-5.25	-5	-4.75	V
Negative supply current	Analog	AIEE		II,IV		170	185	mA
	Digital	DIEE				140	160	mA
Nominal power dissipation		PD		II		3.6	3.7	W
			Full	IV		3.8	3.9	W
Power supply rejection ratio	*(note 2)*	PSRR		IV		+/- 0.5		mV/V
RESOLUTION						8		bits
ANALOG INPUTS								
Full Scale Input Voltage range (differential mode) (0 Volt common mode voltage)		V_{IN}	Full	IV	-125		125	mV
		V_{INB}			-125		125	mV
Full Scale Input Voltage range (single–ended input option) *(see Application Notes)*		V_{IN}	Full	IV	-250		250	mV
		V_{INB}				0		mV
Analog input capacitance		C_{IN}	Full	IV		0.4		pF
Input bias current		I_{IN}	Full	IV		10		µA
Input Resistance		R_{IN}	Full	IV		1		MΩ
Full Power input Bandwidth		FPBW	Full	IV		1.8		GHz
Small Signal input Bandwidth (10 % full scale)		SSBW	Full	IV		1.9		GHz
CLOCK INPUTS								
Logic compatibility for clock inputs *(see Application Notes)*	*(note 10)*				ECL or specified clock input power level in dBm			
ECL Clock inputs voltages (V_{CLK} or V_{CLKB}) :			Full	IV				
• Logic “0” voltage		V_{IL}					-1.5	V
• Logic “1” voltage		V_{IH}			-1.1			V
• Logic “0” current		I_{IL}				5		µA
• Logic “1” current		I_{IH}				5		µA
Clock input power level into 50 Ω termination					DBm into 50 Ω			
Clock input power level			Full	IV	-2	4	10	dBm
Clock input capacitance		C_{CLK}	Full	IV		0.4	3.5	pF

Parameter	Symb	Temp	Test level	Min	Typ	Max	Unit
DIGITAL OUTPUTS (*notes 1,6*)							
Single ended or differential input mode, 50 % clock duty cycle (CLK,CLKB), Binary output data format, Tj (typical) = 70°C. Full temperature range : up to -55°C < Tc ; Tj < +125°C.							
Logic compatibility for digital outputs (Depending on the value of V_{PLUSD}) *(see Application Notes)*				ECL or LVDS			
Differential output voltage swings (assuming V_{PLUSD} = 0V) :		Full	IV				
75 Ω open transmission lines (ECL levels)				1.50	1.620		V
75 Ω differentially terminated				0.70	0.825		V
50 Ω differentially terminated				0.54	0.660		V
Output levels (assuming V_{PLUSD} = 0V) 75 Ω open transmission lines *(note 6)*		25°C	IV				
• Logic “0” voltage	V_{OL}				-1.62	-1.54	V
• Logic “1” voltage	V_{OH}			-0.88	-0.8		V
Output levels (assuming V_{PLUSD} = 0V) 75 Ω differentially terminated *(note 6)*		25°C	IV				
• Logic “0” voltage	V_{OL}				-1.41	-1.34	V
• Logic “1” voltage	V_{OH}			-1.07	-1		V
Output levels (assuming V_{PLUSD} = 0V) 50 Ω differentially terminated *(note 6)*		25°C	II				
• Logic “0” voltage	V_{OL}				-1.35	-1.28	V
• Logic “1” voltage	V_{OH}			-1.09	-1.02		V
Differential Output Swing	DOS	Full	VI	250	290		mV
Output level drift with temperature		Full	IV			1.6	mV/°C
DC ACCURACY							
Single ended or differential input mode, 50 % clock duty cycle (CLK,CLKB), Binary output data format, Tj (typical) = 70°C. Full temperature range :-55°C < Tc ; Tj < +125°C.							
Differential non linearity *(notes 2,3)*	DNL		I		0.4	0.5	LSB
		Full	VI		0.5	0.6	LSB
Integral non linearity *(notes 2,3)*	INL		I		0.7	1	LSB
		Full	VI		0.9	1.2	LSB
No missing codes *(note 3)*		Full	Guaranteed over specified temperature range				
Gain error			I	-10	-2	6	% FS
		Full	VI	-11	-2	7	% FS
Input offset voltage			I	-26	-5	14	mV
		Full	VI	-30	-5	17	mV
Gain error drift		Full	IV	100	125	150	ppm/°C
Offset error drift		Full	IV	40	50	60	ppm/°C

Parameter	Symb	Temp	Test level	Min	Typ	Max	Unit
TRANSIENT PERFORMANCE							
Bit Error Rate *(notes 2, 4)* FS = 1 Gsps Fin = 62.5 MHz	BER	Full	IV			1E-12	Error/ sample
ADC settling time *(note 2)* V_{In} -V_{inB} = 400 mVpp	TS		IV		0.5		ns
Overvoltage recovery time *(note 2)*	ORT		IV		0.5		ns
AC PERFORMANCE							
Single ended or differential input and clock mode, 50 % clock duty cycle (CLK,CLKB), Binary output data format, Tj. = 70°C, unless otherwise specified.							
Signal to Noise and Distortion ratio *(note 2)*	SINAD	Full	IV				
FS = 1 Gsps Fin = 20 MHz				43	45		dB
FS = 1 Gsps Fin = 500 MHz				42	44		dB
FS = 1 Gsps Fin = 1000 MHz (-1dB Fs)				40	42		dB
Effective Number Of bits	ENOB	Full	IV				
FS = 1 Gsps Fin = 20 MHz				7.0	7.2		Bits
FS = 1 Gsps Fin = 500 MHz				6.6	6.8		Bits
FS = 1 Gsps Fin = 1000 MHz (-1dBFs)				6.2	6.4		Bits
Signal to Noise Ratio *(note 2)*	SNR	Full	IV				
FS = 1 Gsps Fin = 20 MHz				42	45		dB
FS = 1 Gsps Fin = 500 MHz				41	44		dB
FS = 1 Gsps Fin = 1000 MHz (-1dBFs)				41	44		dB
Total Harmonic Distortion *(note 2)*	THD	Full	IV				
FS = 1 Gsps Fin = 20 MHz				50	54		dB
FS = 1 Gsps Fin = 500 MHz				46	50		dB
FS = 1 Gsps Fin = 1000 MHz (-1dBFs)				42	46		dB
Spurious Free Dynamic Range *(note 2)*	SFDR	Full	IV				
FS = 1 Gsps Fin = 20 MHz				- 52	- 57		dBc
FS = 1 Gsps Fin = 500 MHz				- 47	- 52		dBc
FS = 1 Gsps Fin = 1000 MHz (-1dBFs)				- 42	- 47		dBc
FS = 1 Gsps Fin = 1000 MHz (-3dBFs)				- 45	- 50		dBc
Two-tone inter-modulation distortion *(note 2)*	IMD	Full	IV				
F_{IN1} = 489 MHz @ F_S = 1 Gsps F_{IN2} = 490 MHz @ F_S = 1 Gsps				- 47	- 52		dBc

Parameter	Symb	Temp	Test level	Min	Typ	Max	Unit
SWITCHING PERFORMANCE AND CHARACTERISTICS – *See Timing Diagrams Figure 1, Figure 2*							
Maximum clock frequency	F_S	Full		1		1.4	GSPS
Minimum clock frequency	F_S	Full	IV		10		MSPS
Minimum Clock pulse width (high)	TC1	Full	IV	0.280	0.500	50	ns
Minimum Clock pulse width (low)	TC2	Full	IV	0.350	0.500	50	ns
Aperture delay *(Note 2)*	TA	Full	IV	100	+250	400	ps
Aperture uncertainty *(Notes 2, 5)*	Jitter	25°C	IV		0.4	0.6	ps (rms)
Data output delay *(Notes 2, 10, 11, 12)*	TOD	Full	IV	1150	1360	1660	ps
Output rise/fall time for DATA (20 % – 80 %) *(note 11)*	TR/TF	Full	IV	250	350	550	ps
Output rise/fall time for DATA READY (20 % – 80 %) *(note 11)*	TR/TF	Full	IV	250	350	550	ps
Data ready output delay *(Notes 2,10, 11, 12)*	TDR	Full	IV	1110	1320	1620	ps
Data ready reset delay	TRDR	Full	IV		720	1000	ps
TOD-TODR *(notes 9, 13)*	TOD-TDR	Full	IV	40	40	40	ps
TC1+TDR-TOD *See Timing Diagram (Note 2) @ 1Gsps*	TD1	Full	IV	460	460	460	ps
Data pipeline delay	TPD	Full	IV		4		clock cycles

Note 1 : Differential output buffers are internally loaded by 75 W resistors. Buffer bias current = 11 mA.

Note 2 : See definition of terms

Note 3 : Histogram testing based on sampling of a 10 MHz sinewave at 50 MSPS.

Note 4 : Output error amplitude < – 4 LSB around worst code.

Note 5 : Maximum jitter value obtained for single–ended clock input on the JTS8388B die (chip on board) : 200 fs. (500 fs expected on JTS8388B)

Note 6 : Digital output back termination options depicted in Application Notes figures 3,4,5 .

Note 7 : With a typical value of TD = 465 ps, at 1 Gsps, the timing safety margin for the data storing using the ECLinPS 10E452 output registers from Motorola is of – 315 ps, equally shared before and after the rising edge of the Data Ready signals (DR, DRB).

Note 8 : The clock inputs may be indifferently entered in differential or single–ended, using ECL levels or 4 dBm typical power level into the 50 W termination resistor of the inphase clock input.
(4 dBm into 50 W clock input correspond to 10 dBm power level for the clock generator.)

Note 9 : At 1GSPS, 50/50 clock duty cycle, TC2 = 500 ps (TC1). TDR - TOD = -100 ps (typ) does not depend on the sampling rate.

Note 10 : Specified loading conditions for digital outputs :
- 50 W or 75 W controlled impedance traces properly 50 / 75 W terminated, or unterminated 75 W controlled impedance traces.
- Controlled impedance traces far end loaded by 1 standard ECLinPS register from Motorola.(e.g. : 10E452) (Typical input parasitic capacitance of 1.5 pF including package and ESD protections.)

Note 11 : Termination load parasitic capacitance derating values :
- 50 W or 75 W controlled impedance traces properly 50 / 75 W terminated : 60 ps / pF or 75 ps per additionnal ECLinPS load.
- Unterminated (source terminated) 75 W controlled impedance lines : 100 ps / pF or 150 ps per additionnal ECLinPS termination load.

Note 12 : apply proper 50 / 75 impedance traces propagation time derating values : 6 ps / mm (155 ps/inch) for TSEV8388B Evaluation Board.

Note 13 : Values for TOD and TDR track each other over temperature, (1 % variation for TOD - TDR per 100 °C. temperature variation). Therefore TOD - TDR variation over temperature is negligible. Moreover, the internal (onchip) and package skews between each Data TODs and TDR effect can be considered as negligible.Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values (see Advanced Application Notes about TOD - TDR variation over temperature in section 7).

3.4. TIMING DIAGRAMS

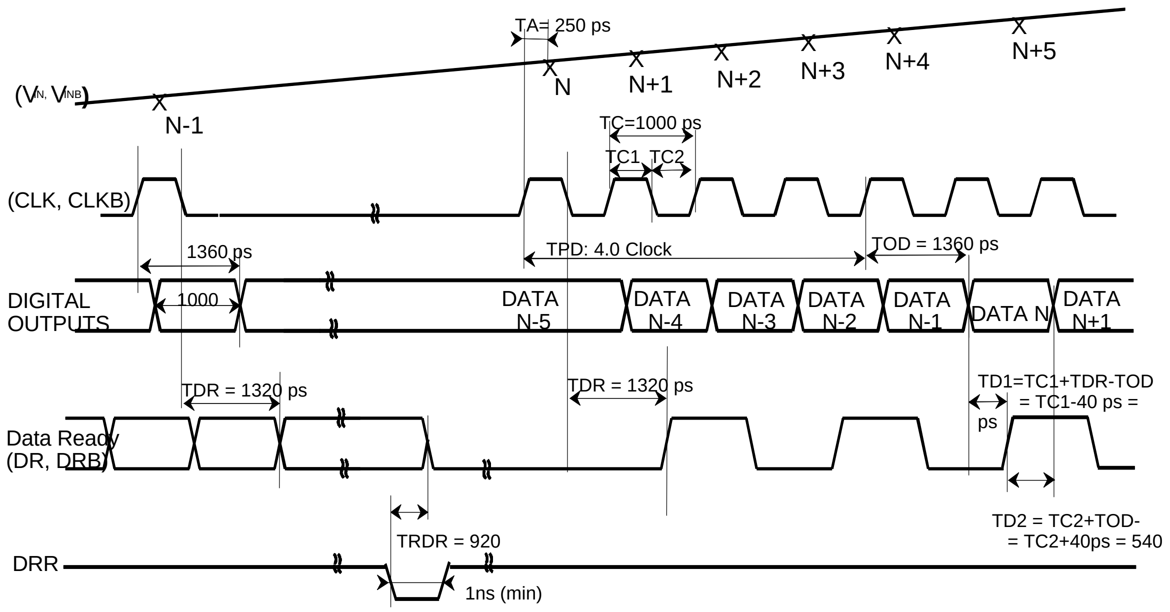


Figure 1 **JTS8388B TIMING DIAGRAM (1 GSPS CLOCK)**

Data Ready Reset , Clock held at LOW

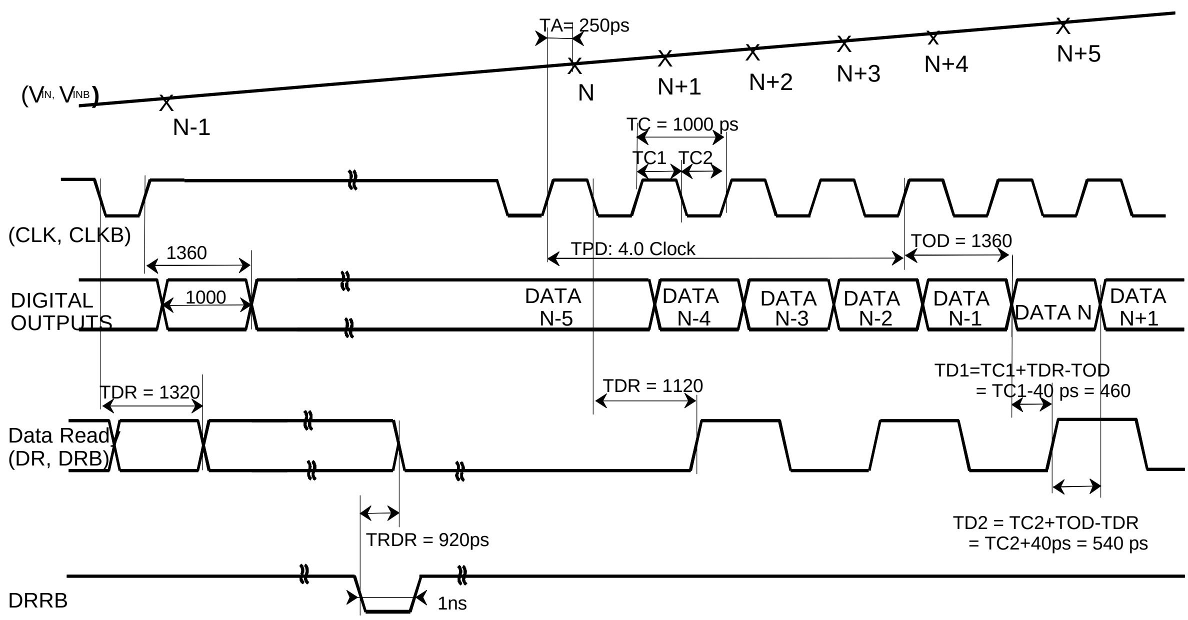


Figure 2 **JTS8388B TIMING DIAGRAM (1 GSPS CLOCK)**

Data Ready Reset , Clock held at HIGH

3.5. EXPLANATION OF TEST LEVELS

D	100 % wafer tested at +25°C [(1)]
I	100% production tested at +25°C [(1)] (for packaged device).
II	100 % production tested at +25°C [(1)], and sample tested at specified temperatures
III	Sample tested only at specified temperatures
IV	Parameter is guaranteed by design and characterization testing (thermal steady-state conditions at specified temperature).
V	Parameter is a typical value only
VI	100 % production tested over specified temperature range.

Only MIN and MAX values are guaranteed (typical values are issuing from characterization results).

[(1)] *Unless otherwise specified, all tests are pulsed tests : therefore Tj = Tc = Ta,*

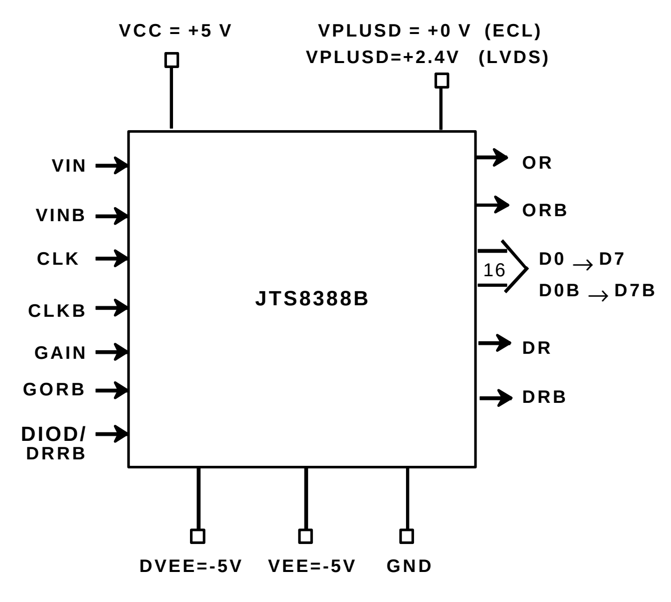
3.6. WAFER SCREENING

Parameter	Temperature	JTS8388B chip		Unit
		Min	Max	
DC Accuracy @ 50 MSPS / 10 MHz	25°C [(2)]			
DNL				LSB
INL				LSB
No missing codes		Guaranteed		
AC Performance TBD	25°C [(2)]			
SNR		45		dB
ENOB		7.1		bit

[(2)] *Unless otherwise specified, all tests are pulsed tests : therefore Tj = Tc = Ta,*

3.7. FUNCTIONS DESCRIPTION

Name	Function
VCC	Positive power supply
VEE	Analog negative power supply
VPLUSD	Digital positive power supply
GND	Ground
VIN, VINB	Differential analog inputs
CLK, CLKB	Differential clock inputs
<D0:D7> <D0B:D7B>	Differential output data port
DR ; DRB	Differential data ready outputs
OR ; ORB	Out of range outputs
GAIN	ADC gain adjust
GORB	Gray or Binary digital output select
DIOD/DRRB	Die junction temp. measurement/ asynchronous data ready reset



3.8. DIGITAL OUTPUT CODING

NRZ (Non Return to Zero) mode, ideal coding : does not include gain, offset, and linearity voltage errors.

Differential analog input	Voltage level	Digital output		Out of Range
		Binary GORB = VCC or floating	Gray GORB = GND	
> +251 mV	> Positive full scale + 1/2 LSB	1 1 1 1 1 1 1 1	1 0 0 0 0 0 0 0	1
+251 mV +249 mV	Positive full scale + 1/2 LSB Positive full scale – 1/2 LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	1 0 0 0 0 0 0 0 1 0 0 0 0 0 0 1	0 0
+126 mV +124 mV	Positive 1/2 scale + 1/2 LSB Positive1/2 scale – 1/2 LSB	1 1 0 0 0 0 0 0 1 0 1 1 1 1 1 1	1 0 1 0 0 0 0 0 1 1 1 0 0 0 0 0	0 0
+1 mV -1 mV	Bipolar zero + 1/2 LSB Bipolar zero - 1/2 LSB	1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1	1 1 0 0 0 0 0 0 0 1 0 0 0 0 0 0	0 0
-124 mV -126 mV	Negative 1/2 scale + 1/2 LSB Negative 1/2 scale - 1/2 LSB	0 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1	0 1 1 0 0 0 0 0 0 0 1 0 0 0 0 0	0 0
-249 mV -251 mV	Negative full scale + 1/2 LSB Negative full scale - 1/2 LSB	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0
< -251 mV	< Negative full scale - 1/2 LSB	0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	1

4. PACKAGE DESCRIPTION.

4.1. JTS8388B PIN DESCRIPTION

Symbol	Pin number	Function
GND	20, 24, 26, 28, 33, 35, 37	Analog ground. Pads n°20, 24,26,28,37 are double. Pads n°26,33,35 are single. 14 bonding wires are available for analog ground access.
V_{PLUSD}	1, 11	Digital positive supply. (0V for ECL compatibility, +2.4V for LVDS compatibility). 2 double pads *(note 3)*
V_{CC}	19, 21, 23, 30, 39, 40	+5 V positive supply.
V_{EE}	22, 29, 31	-5 V analog supply.
DV_{EE}	6	-5 V digital supply.
V_{IN}	34	In phase (+) analog input signal of the Sample and Hold differential preamplifier.
V_{INB}	36	Inverted phase (-) of analog input signal.
CLK	25	In phase (+) ECL clock input.
CLKB	27	Inverted phase (-) of ECL clock input.
D0, D1, D2, D3, D4, D5, D6, D7	16, 14, 12, 9, 4, 2, 45, 43	In phase (+) digital outputs. D0 is the LSB. D7 is the MSB.
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B	17, 15, 13, 10, 5, 3, 46, 44	Inverted phase (-) Digital outputs. B0B is the inverted LSB. D7B is the inverted MSB.
OR	41	In phase (+) Out of Range Output. Out of Range goes high on the leading edge of code 0 and code 256.
ORB	42	Inverted phase (+) of Out of Range Bit (OR).
DR	7	In phase (+) output of Data Ready Signal.
DRB	8	Inverted phase (-) output of Data Ready Signal.
GORB	18	Gray or Binary select output format control pad. – Binary output format if GORB is floating or V_{CC}. – Gray output format if GORB is connected at ground (0 V).
GAIN	38	ADC gain adjust pin.
DIOD/DRRB	32	DIOD : die junction temperature measurement pad. Can be left floating or grounded if not used. DRRB : asynchronous data ready reset function

4.2. JTS8388B CHIP PAD LIST, COORDINATES AND CORRESPONDING FUNCTIONS

Pad number	PosX	PosY	Chip pad function	
1	880	1365	V_{PLUSD}	Positive digital supply (double pad) (note 3)
2	670	1365	D5	In phase (+) digital output, bit 5 (D7 is the MSB ; Bit 7, D0 is the LSB ; Bit 0)
3	510	1365	D5B	Inverted phase (-)digital output, bit 5
4	350	1365	D4	In phase (+) digital output, bit 4
5	190	1365	D4B	Inverted phase (-) digital output, bit 4
6	-20	1365	DV_{EE}	-5V digital supply (double pad)
7	-230	1365	DR	In phase (+) Data Ready
8	-390	1365	DRB	Inverted Phase (-) Data Ready
9	-550	1365	D3	In phase (+) digital output, bit 3
10	-710	1365	D3B	Inverted phase (-) digital output, bit 3
11	-920	1365	V_{PLUSD}	Positive digital supply (double pad) (note 3)
12	-1085	1115	D2	In phase (+) digital output, bit 2
13	-1085	955	D2B	Inverted phase (-) digital output, bit 2
14	-1085	795	D1	In phase (+) digital output, bit 1
15	-1085	635	D1B	Inverted phase (-) digital output, bit 1
16	-1085	475	D0	In phase (+) digital output, bit 0, Least Significant Bit
17	-1085	315	D0B	Inverted phase (-) digital output, bit 0, Least Significant Bit
18	-1085	155	GORB	Gray or Binary data output format select. (Note 2)
19	-1085	-55	V_{CC}	+5V supply (double pad)
20	-1085	-325	GND	Analog Ground (double pad)
21	-1085	-595	V_{CC}	+5V supply (double pad)
22	-1085	-865	V_{EE}	-5V analog supply (double pad)
23	-1085	-1135	V_{CC}	+5V supply (double pad)
24	-905	-1365	GND	Analog Ground (double pad)
25	-655	-1365	CLK	In phase (+) clock input (double pad)
26	-455	-1365	GND	Analog Ground
27	-255	-1365	CLKB	Inverted phase (-) clock input (double pad)
28	-5	-1365	GND	Analog Ground (double pad)
29	245	-1365	V_{EE}	-5V analog supply (double pad)
30	495	-1365	V_{CC}	+5V supply (double pad)
31	745	-1365	V_{EE}	-5V analog supply (double pad)
32	945	-1365	DIOD/DRRB	Diode input for Tj monitoring / Input for asynchronous Data Ready Reset
33	1085	-1195	GND	Analog Ground
34	1085	-995	V_{IN}	In phase (+) analog input (double pad)
35	1085	-795	GND	Analog Ground
36	1085	-595	$V_{IN}B$	Inverted phase (-) analog input (double pad)
37	1085	-345	GND	Analog Ground (double pad)
38	1085	-145	GAIN	ADC gain adjust input
39	1085	55	V_{CC}	+5V supply (double pad)
40	1085	265	V_{CC}	+5V supply
41	1085	425	OR	In phase (+) Out of Range digital output
42	1085	585	ORB	Inverted phase (-) Out of Range digital output
43	1085	745	D7	In phase (+) digital output, bit 7, Most Significant Bit
44	1085	905	D7B	Inverted phase (-) digital output bit 7
45	1085	1065	D6	In phase (+) digital output, bit 6
46	1085	1225	D6B	Inverted phase (-) digital output, bit 6

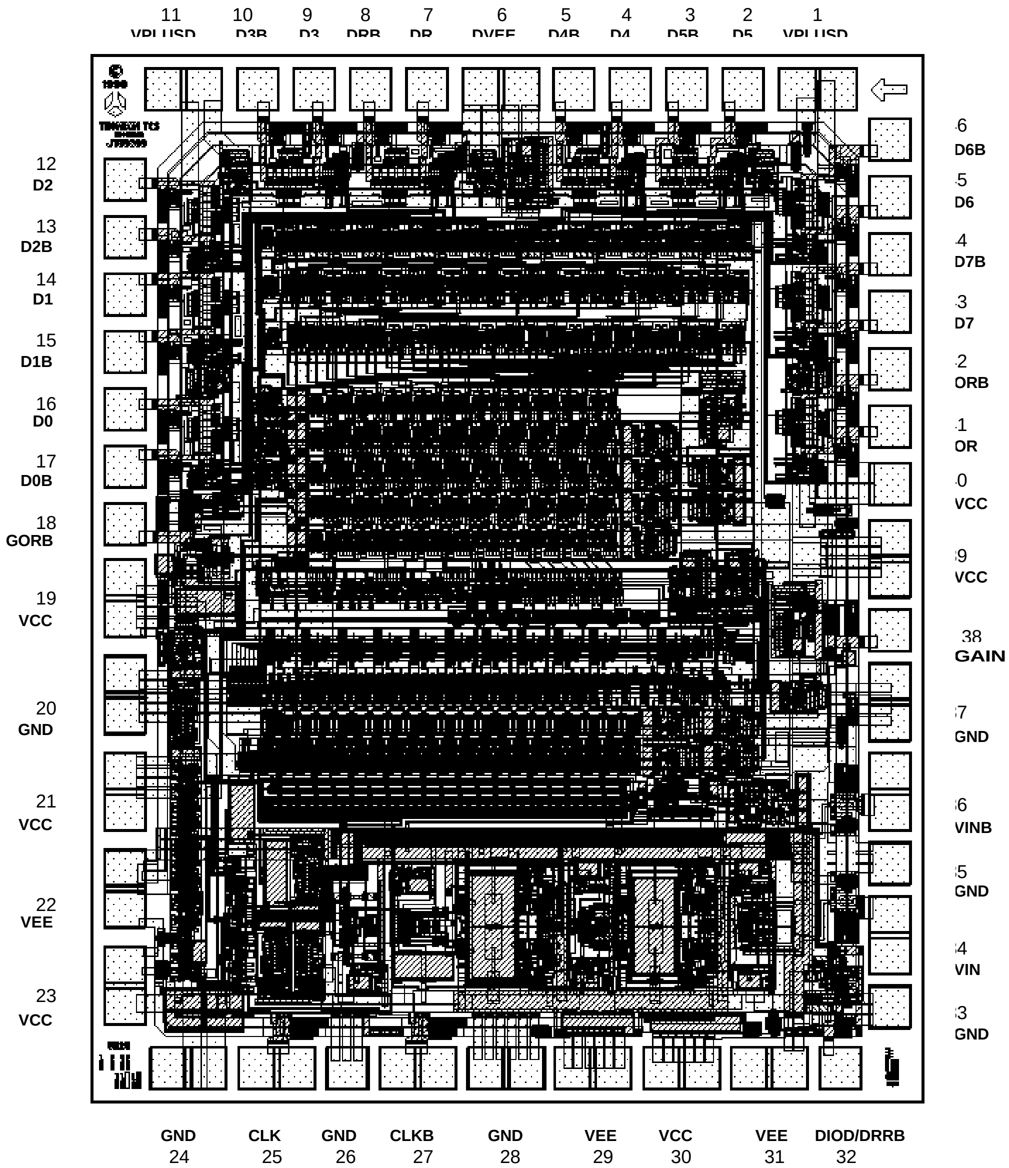
Note 1 : Coordinates are relative to pad centers. The coordinates origin (0,0) is at the center of the die.
All dimensions are given in microns. The pad 1 is the one pointed at by the arrow (see layout).
Distance between pad (glass window) and inner edge of seal-ring : 40µm.
Die size (inner edge of seal-ring : (-1175, -1175, 1455).
Die size (including scribe line) : (-1230, -1510) (1230, 1510) (2.46 x 3.02 mm²).
Actual die size (after separation) : (-1220, -1500) (1220, 1500) (2.44 mm x 3.00 mm).

Note 2 : GORB tied to Vcc or floating : Binary output data format. GORB tied to GND : Gray output data format

Note3 : The common mode level of the output buffers is 1.2V below the positive digital supply.
For ECL compatibility the positive digital supply must be set at 0V (ground).
For LVDS compatibility (output common mode at +1.2V) the positive digital supply must be set at 2.4V.
If the subsequent LVDS circuitry can withstand a lower level for input common mode, it is recommended to lower the positive digital supply level in the name proportion in order to spare power dissipation.

4.3. JTS8388B CHIP PADS DESIGNATION VH25B

Die Size : 2.44 x 3.00 mm (after separation) Die Area : 7.32 mm²



4.4. DIE MECHANICAL INFORMATIONS

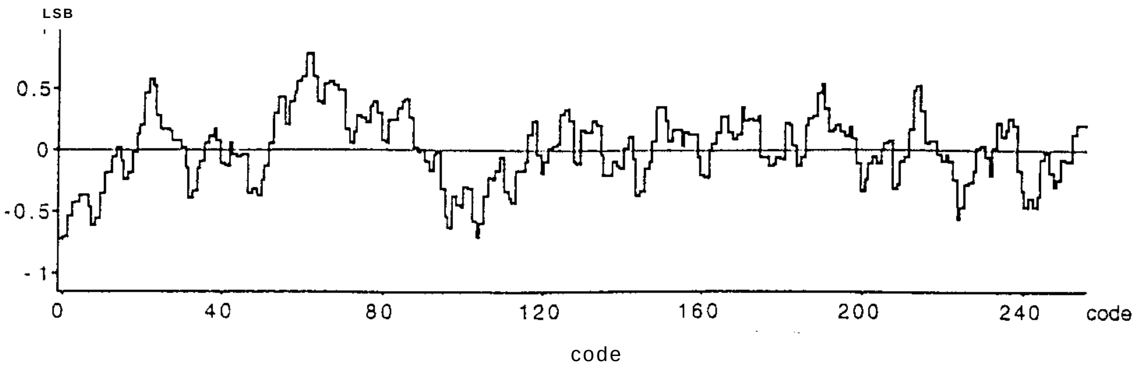
Mask reference		VH25B
Die size	between scribe line axis	2.46 mm x 3.02 mm
	after separation	2.44 mm x 3.00 mm
Prad size	(single pad)	100 µm x 100 µm
	(double pad)	200 µm x 100 µm
Die thickness		300 µm ± 20 µm
Back side metallization		none
Metallization	Number of layers	3
	Material	Ti/TiN Al-Si-Cu TiN (on top)
	Diffusion barrier	Ti/TiN
	Thickness	Metal 1 : 600 nm : Metal 2 & Metal 3 : 800 nm
Pad metallization (1) (2)		Ti/TiN Al-Si-Cu TiN (Metal 2)
		Ti/TiN Al-Si-Cu TiN (Metal 3)
Passivation		Oxide/Nitride (SiO_2/SiN_2) : 300nm / 550 nm
Back side potential		-5V
Die transistor count		4450
Die attach		epoxy Ag filled high conductivity glue
Bond wire		Al or Au 30 µm diameter
Qualification package		CQFP68 (with restriction on electrical performance)

Note 1 : The top TiN layer is etched in one step together with the passivation layer.
Note 2 : The pad is a sandwich of Metal 2 and Metal 3 over field oxyde.

5. TYPICAL CHARACTERIZATION RESULTS

5.1. STATIC LINEARITY – FS = 50 MSPS / FIN = 10 MHZ

5.1.1. INTEGRAL NON LINEARITY

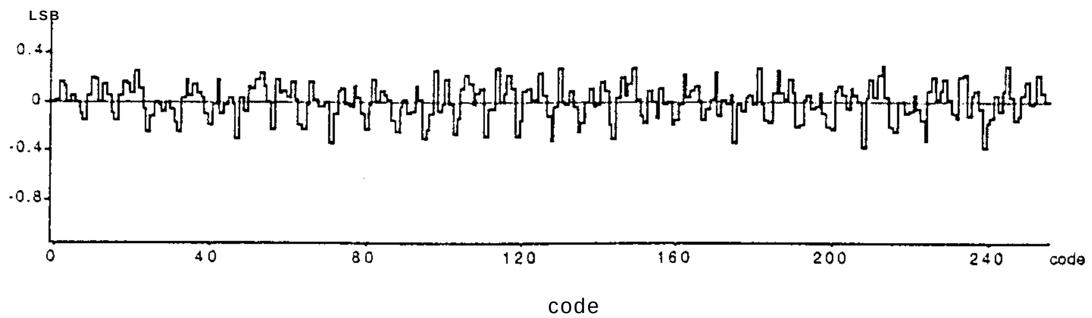


INL = +/- 0.7 LSB

Clock Frequency = 50Msps Signal Frequency = 10MHz

Positive peak : 0.78 LSB Negative peak : -0.73 LSB

5.1.2. DIFFERENTIAL NON LINEARITY

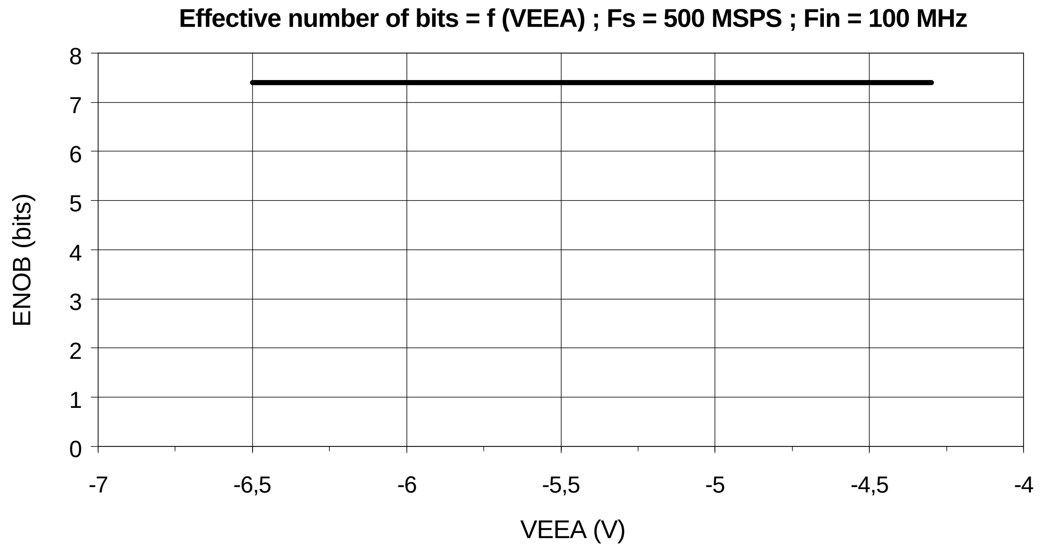


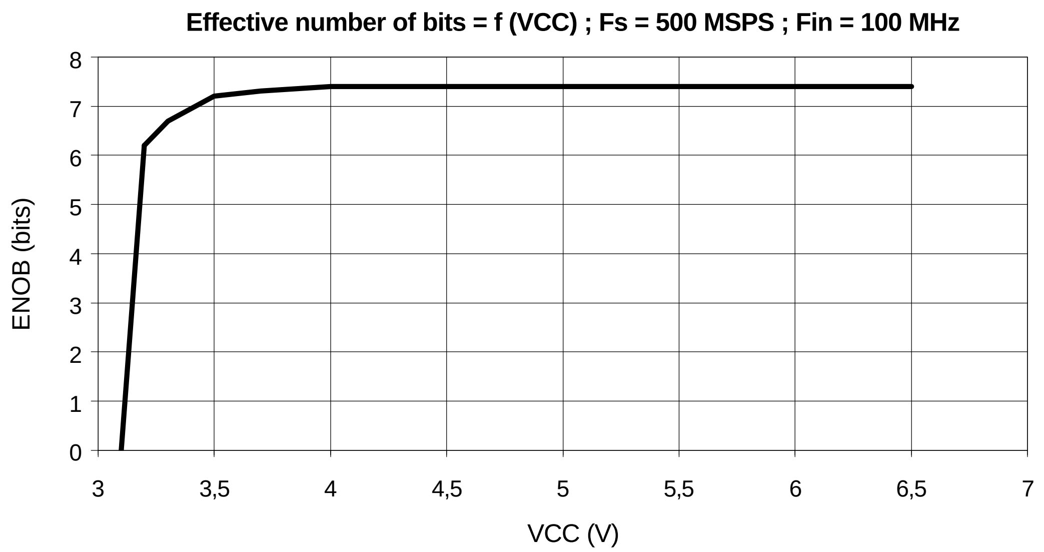
DNL = +/- 0.4 LSB

Clock Frequency = 50Msps Signal Frequency = 10MHz

Positive peak : 0.3 LSB Negative peak : -0.39 LSB

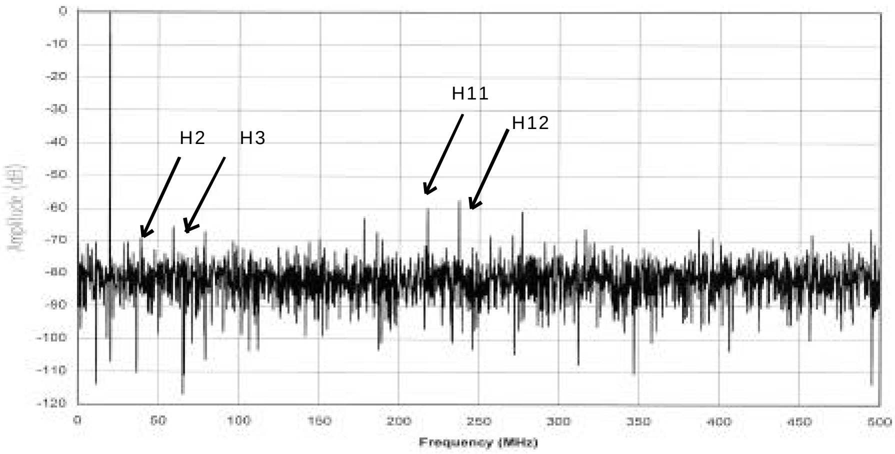
5.2. EFFECTIVE NUMBER OF BITS VERSUS POWER SUPPLIES VARIATION





5.3. TYPICAL FFT RESULTS

5.3.1. FS = 1 GSPS, FIN=20 MHZ



Single Ended or differential

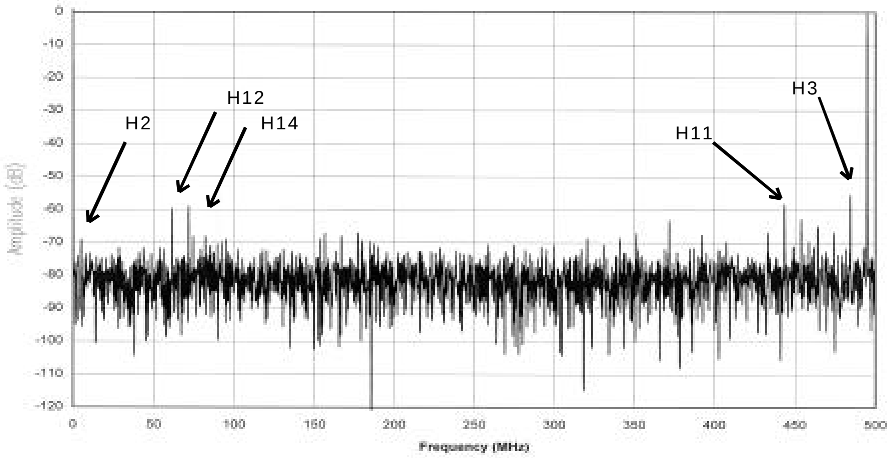
Fs =1 GSPS
Fin = 20 MHz

Eff. Bits =7.2
SINAD = 45 dB
SNR = 45 dB
THD = -54 dBc
SFDR = -57 dBc

Binary output coding

clock duty cycle = 50 %

5.3.2. FS = 1 GSPS, FIN = 495 MHZ



Single Ended or differential

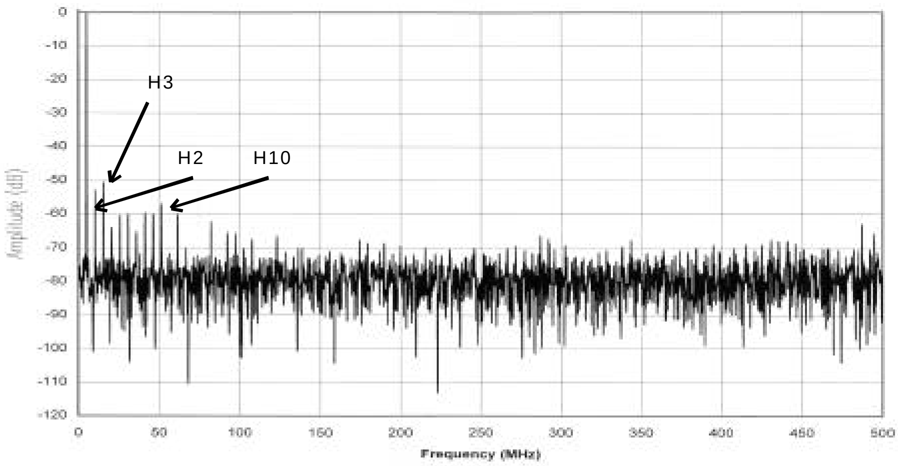
Fs =1 GSPS
Fin=495MHz

Eff. Bits =6.8
SINAD = 44 dB
SNR = 44 dB
THD = -50 dBc
SFDR= -52 dBc

Binary output coding

clock duty cycle = 50 %

5.3.3. FS = 1 GSPS, FIN = 995 MHZ (-3DB FULL SCALE INPUT)



Single Ended or differential

Fs =1 GSPS
Fin=995 MHz

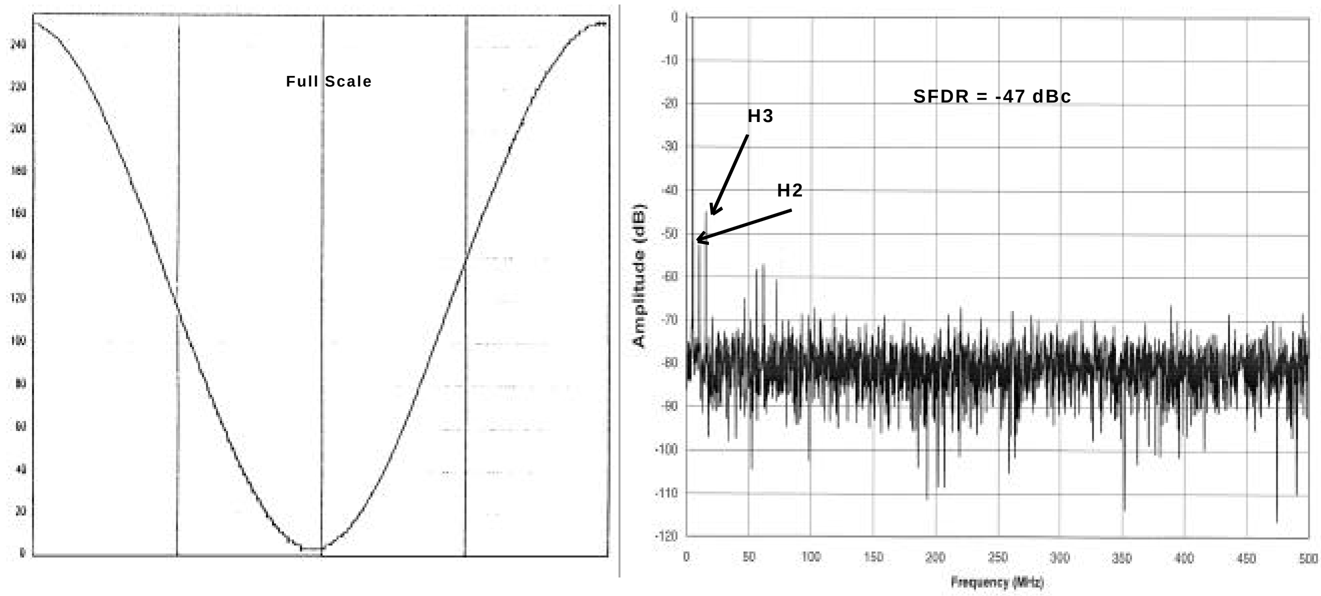
Eff. Bits =6.4
SINAD =42 dB
SNR = 44 dB
THD = -46 dBc
SFDR= -50 dBc

Binary output coding

clock duty cycle = 50 %

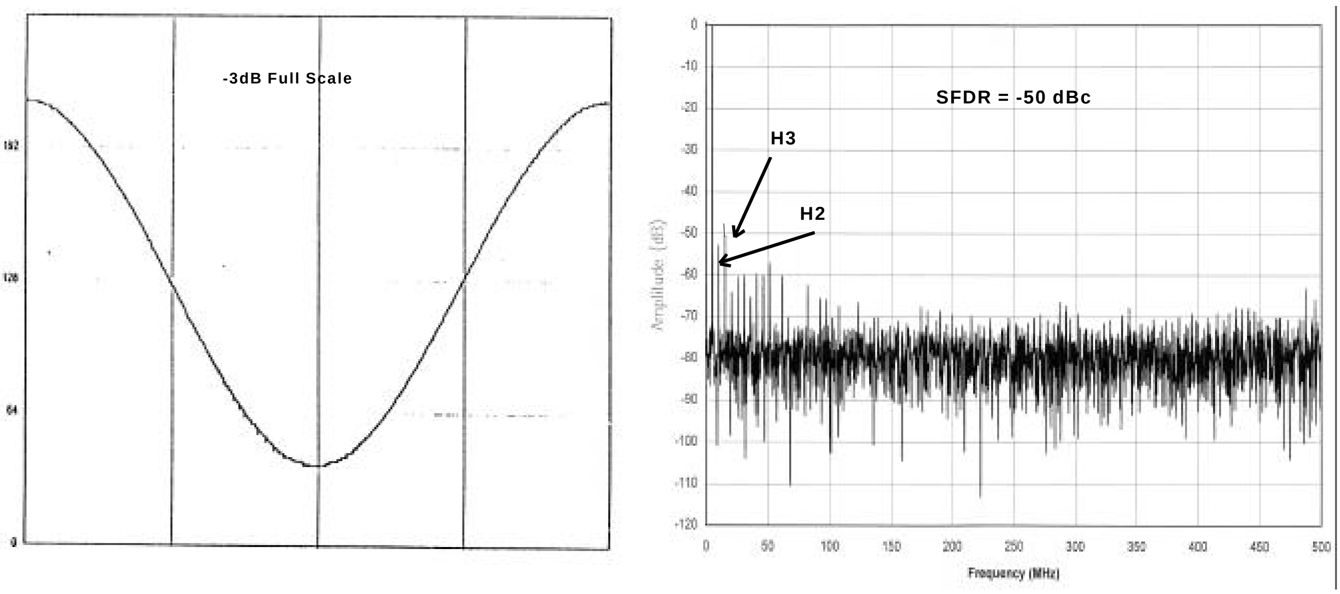
5.4. SPURIOUS FREE DYNAMIC RANGE VERSUS INPUT AMPLITUDE

5.4.1. SAMPLING FREQUENCY FS=1 GSPS ; INPUT FREQUENCY FIN=995 MHZ ; GRAY OR BINARY OUTPUT CODING



Fs = 1 GSPS Fin = 995 MHz Full Scale

ENOB = 6.4 SINAD = 42 dB SNR = 44 dB THD = 46 dBc SFDR = -47 dBc

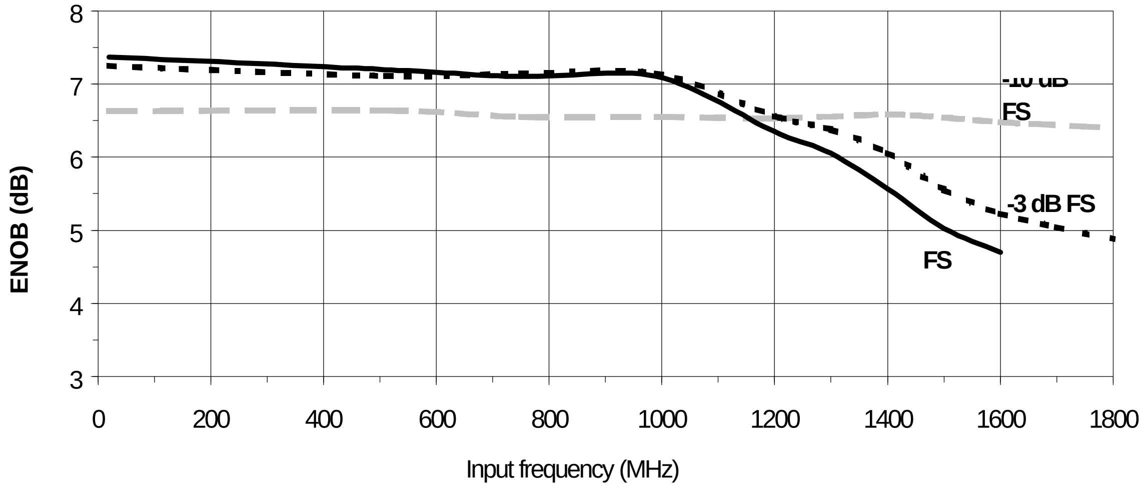


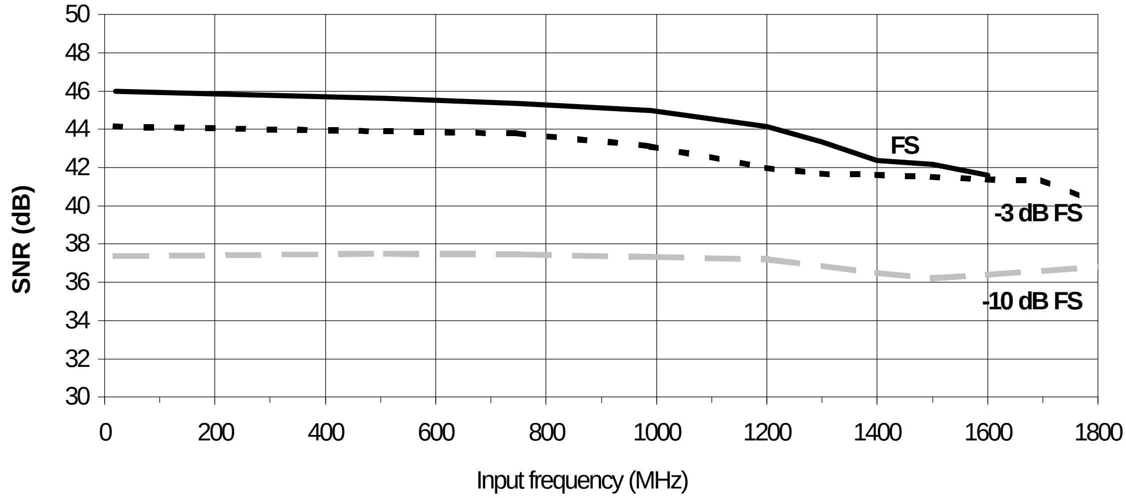
Fs = 1 GSPS Fin = 995 MHz (-3 dB Full Scale)

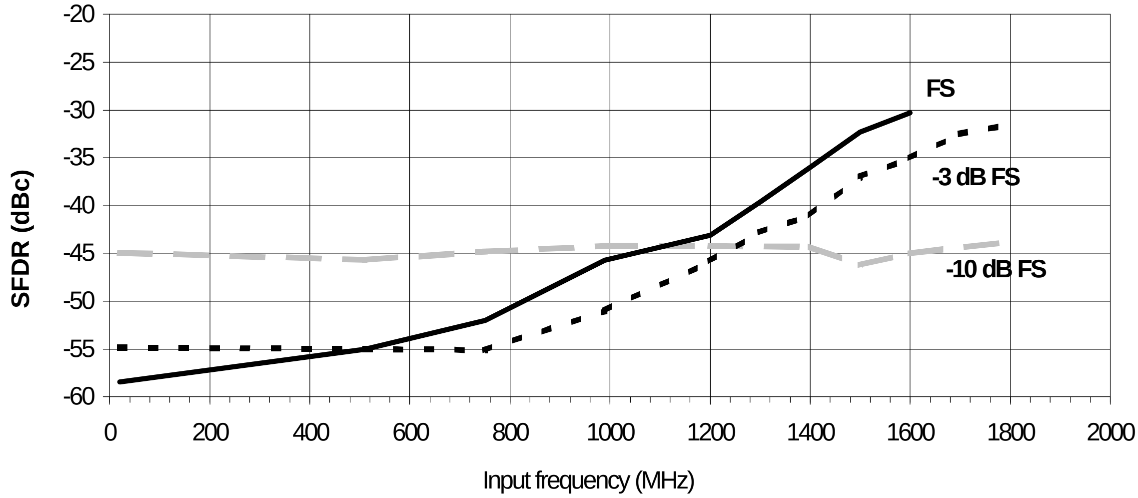
ENOB = 6.6 SINAD = 43 dB SNR = 44 dB THD = -48 dBc SFDR = -50 dBc

5.5. DYNAMIC PERFORMANCE VERSUS ANALOG INPUT FREQUENCY

Fs=1 Gsps, Fin = 0 up to 1600 MHz, Full Scale input (FS), FS -3 dB
Clock duty cycle 50 / 50, Binary/Gray output coding, fully differential or single-ended analog and clock inputs

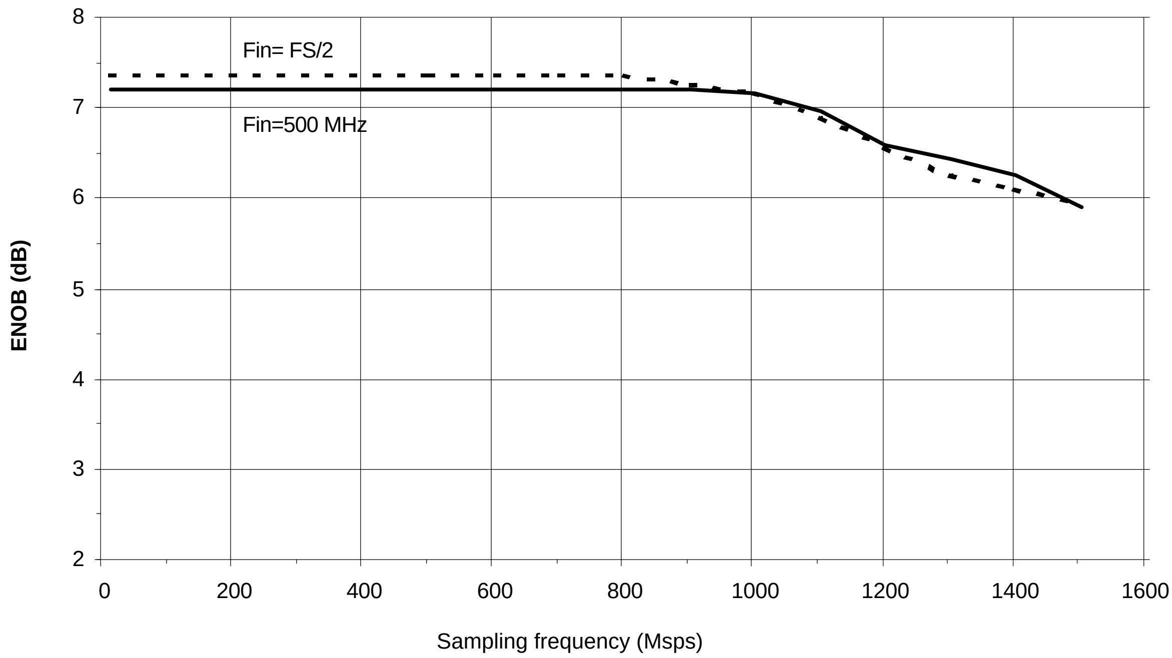






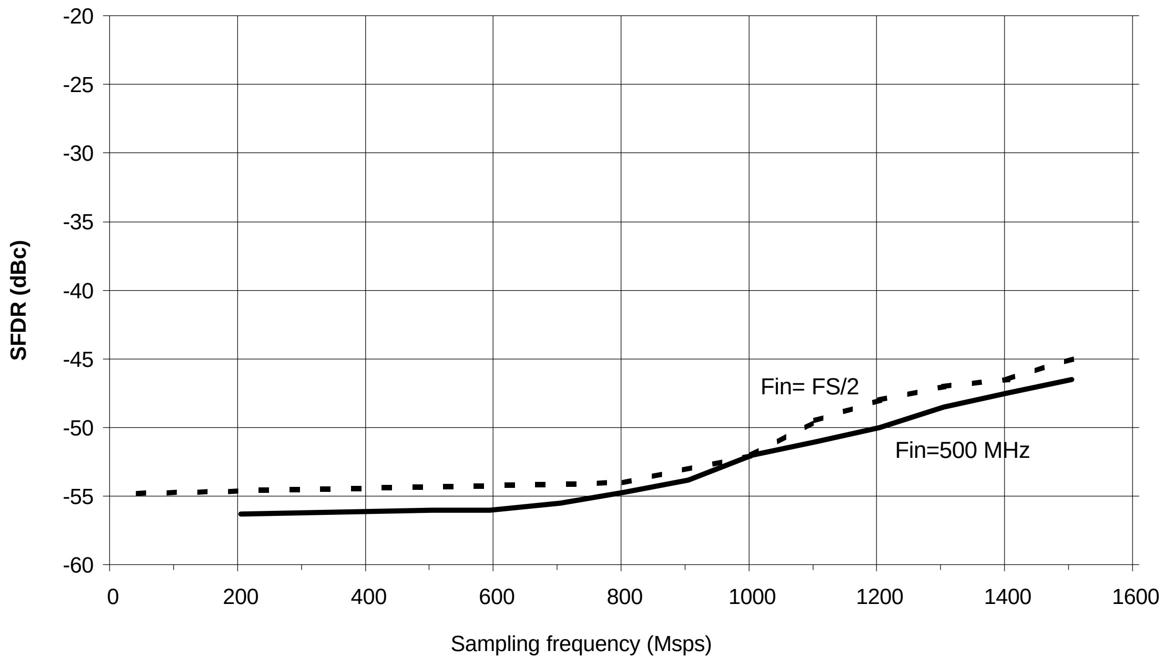
5.6. EFFECTIVE NUMBER OF BITS (ENOB) VERSUS SAMPLING FREQUENCY

Analog Input Frequency : Fin = 495 MHz and Nyquist conditions (Fin = Fs / 2)
Clock duty cycle 50 / 50 , Binary output coding

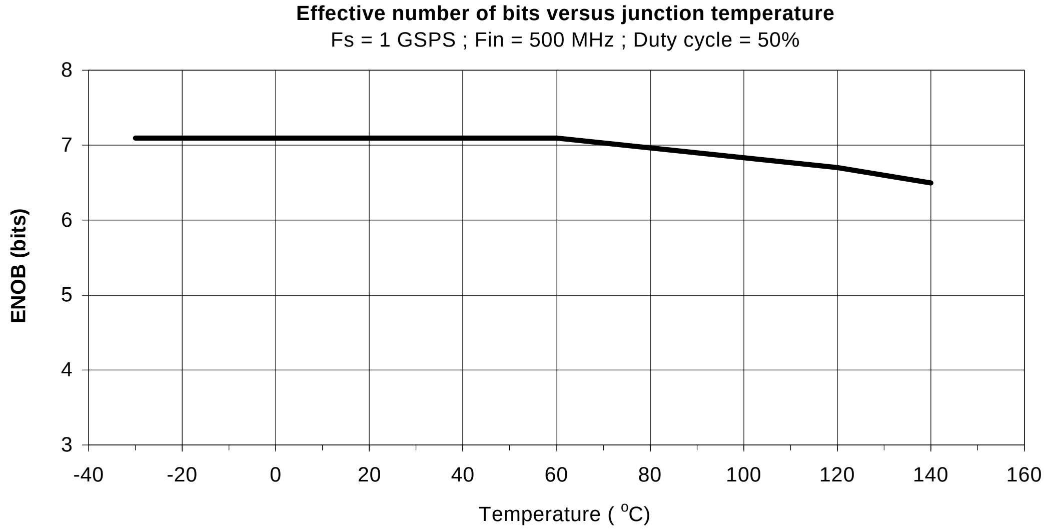


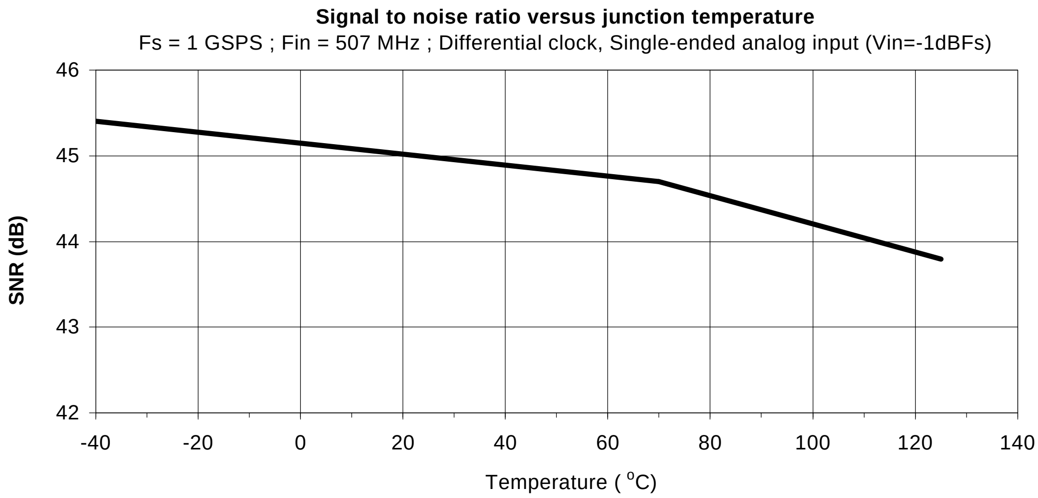
5.7. SFDR VERSUS SAMPLING FREQUENCY

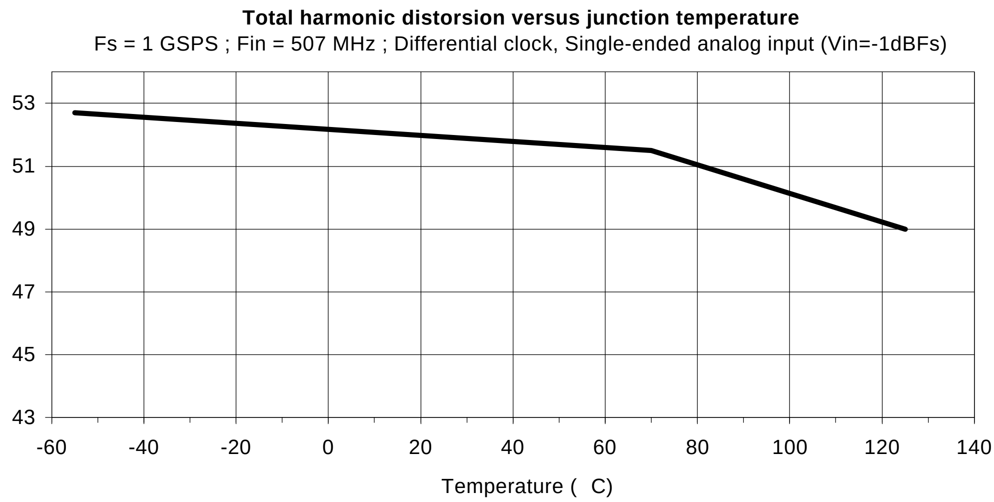
Analog Input Frequency : Fin = 495 MHz and Nyquist conditions (Fin = Fs / 2)
Clock duty cycle 50 / 50 , Binary output coding

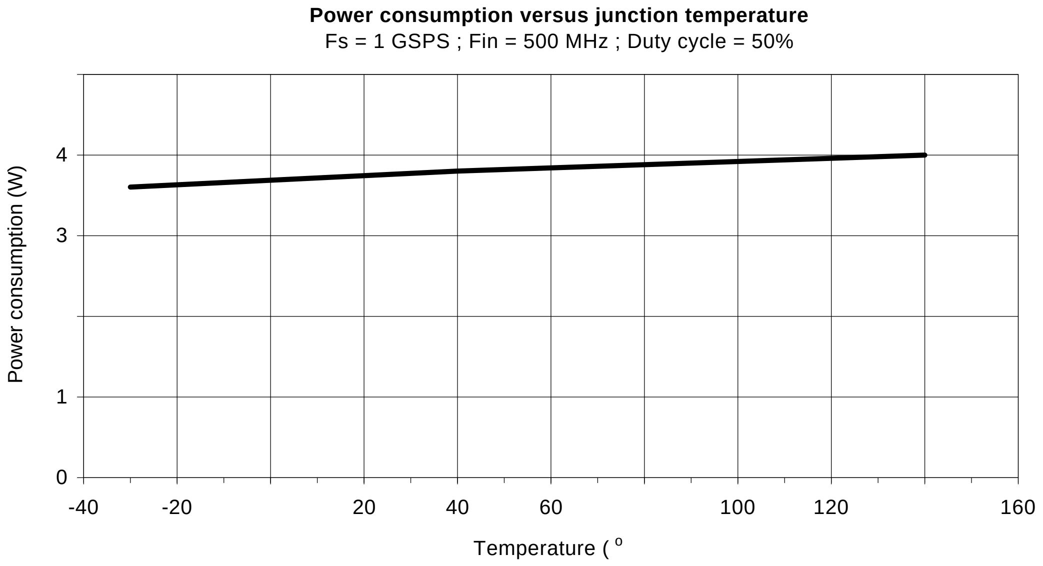


5.8. JTS8388B ADC PERFORMANCES VERSUS JUNCTION TEMPERATURE



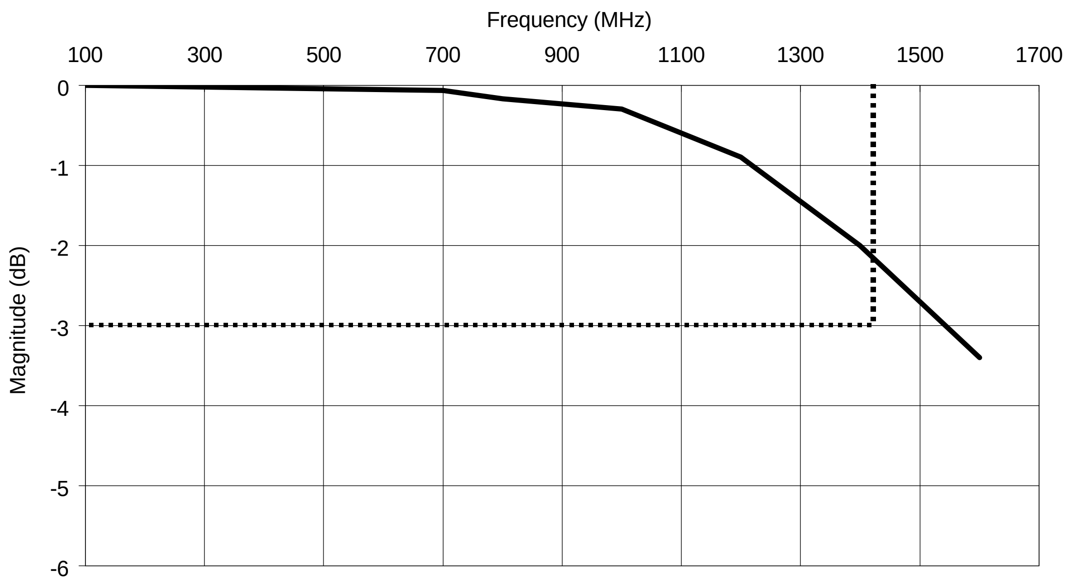






5.9. TYPICAL FULL POWER INPUT BANDWIDTH

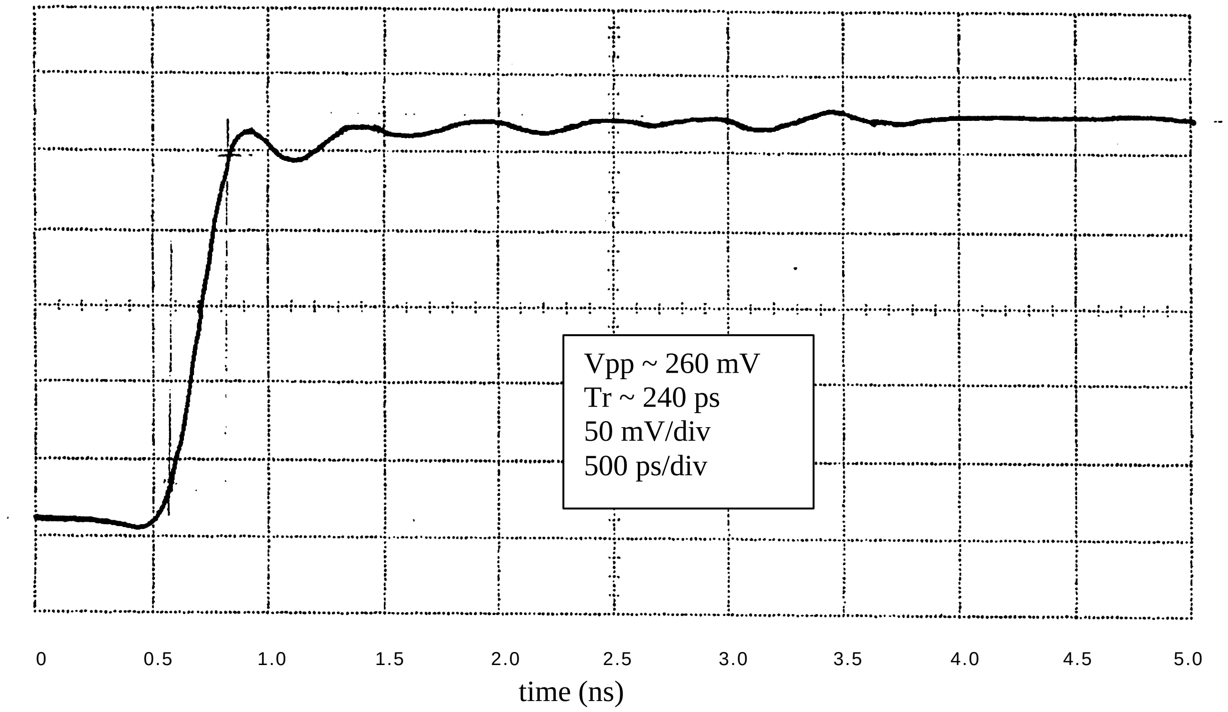
at -3 dB (-2dBm full power input)



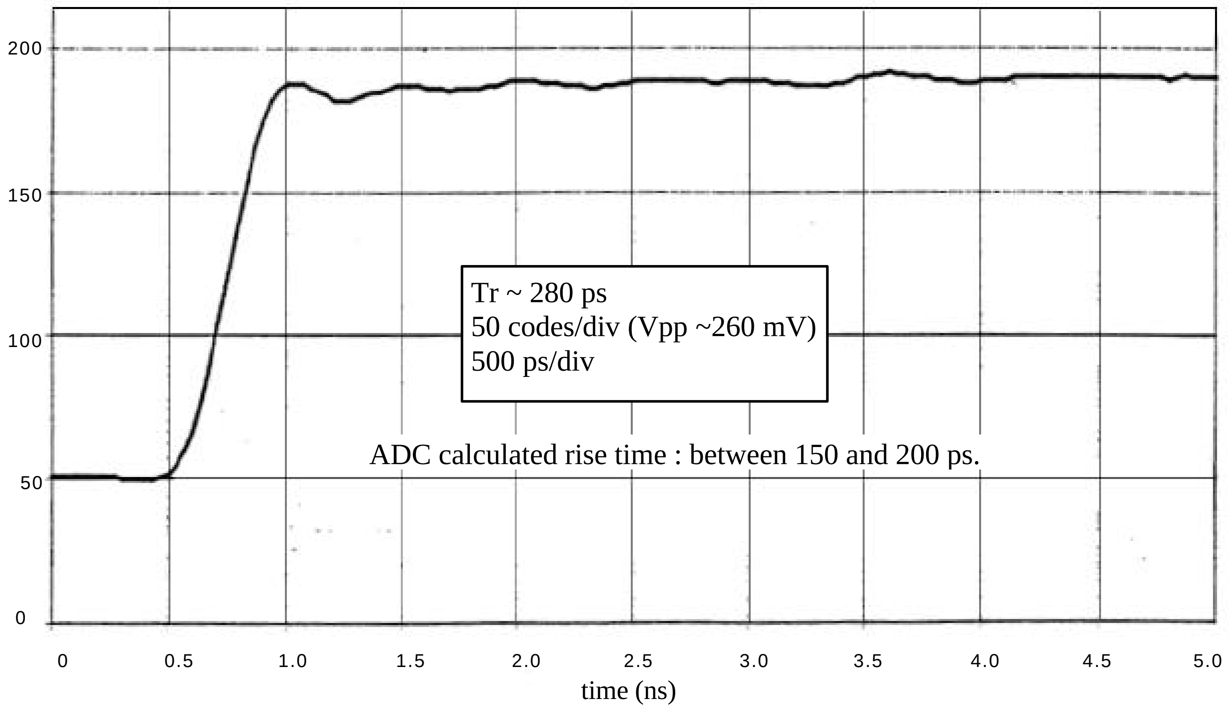
5.10. ADC STEP RESPONSE

Test pulse input characteristics : 20% to 80% input full scale and rise time ~ 200ps.

5.10.1. TEST PULSE DIGITIZED WITH 20 GHZ DSO



5.10.2. SAME TEST PULSE DIGITIZED WITH JTS8388B ADC



N.B. : ripples are due to the test setup (they are present on both measurements)

6. DEFINITION OF TERMS

(BER)	*Bit Error Rate*	Probability to exceed a specified error threshold for a sample. An error code is a code that differs by more than +/- 4 LSB from the correct code.
(BW)	*Full power input bandwidth*	Analog input frequency at which the fundamental component in the digitally reconstructed output has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at Full Scale.
(SINAD)	*Signal to noise and distortion ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale, to the RMS sum of all other spectral components, including the harmonics except DC.
(SNR)	*Signal to noise ratio*	Ratio expressed in dB of the RMS signal amplitude, set to 1dB below Full Scale, to the RMS sum of all other spectral components excluding the five first harmonics.
(THD)	*Total harmonic distortion*	Ratio expressed in dBc of the RMS sum of the first five harmonic components, to the RMS value of the measured fundamental spectral component.
(SFDR)	*Spurious free dynamic range*	Ratio expressed in dB of the RMS signal amplitude, set at 1dB below Full Scale, to the RMS value of the next highest spectral component (peak spurious spectral component). SFDR is the key parameter for selecting a converter to be used in a frequency domain application (Radar systems, digital receiver, network analyzer ....). It may be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (i.e. always related back to converter full scale).
(ENOB)	*Effective Number Of Bits*	$ENOB = \dfrac{SINAD - 1.76 + 20 \log (A/V/2)}{6.02}$ Where A is the actual input amplitude and V is the full scale range of the ADC under test
(DNL)	*Differential non linearity*	The Differential Non Linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic.
(INL)	*Integral non linearity*	The Integral Non Linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs, and is the maximum value of all |INL (i)|.
(DG)	*Differential gain*	The peak gain variation (in percent) at five different DC levels for an AC signal of 20% Full Scale peak to peak amplitude. F_{IN} = 5 MHz. (TBC)
(DP)	*Differential phase*	Peak Phase variation (in degrees) at five different DC levels for an AC signal of 20% Full Scale peak to peak amplitude. F_{IN} = 5 MHz. (TBC)
(TA)	*Aperture delay*	Delay between the rising edge of the differential clock inputs (CLK,CLKB) (zero crossing point), and the time at which (V_{IN},V_{INB}) is sampled.
(JITTER)	*Aperture uncertainty*	Sample to sample variation in aperture delay. The voltage error due to jitter depends on the slew rate of the signal at the sampling point.
(TS)	*Settling time*	Time delay to achieve 0.2 % accuracy at the converter output when a 80% Full Scale step function is applied to the differential analog input.
(ORT)	*Overvoltage recovery time*	Time to recover 0.2 % accuracy at the output, after a 150 % full scale step applied on the input is reduced to midscale.
(TOD)	*Digital data Output delay*	Delay from the falling edge of the differential clock inputs (CLK,CLKB) (zero crossing point) to the next point of change in the differential output data (zero crossing) with specified load.
(TD1)	*Time delay from Data to Data Ready*	Time delay from Data transition to Data ready.
(TD2)	*Time delay from Data Ready to Data*	General expression is TD1 = TC1 + TDR - TOD with TC = TC1 + TC2 = 1 encoding clock period.
(TC)	*Encoding clock period*	TC1 = Minimum clock pulse width (high) TC = TC1 + TC2 TC2 = Minimum clock pulse width (low)
(TPD)	*Pipeline Delay*	Number of clock cycles between the sampling edge of an input data and the associated output data being made available, (not taking in account the TOD). For the JTS8388B the TPD is 4 clock periods.

(TRDR)	*Data Ready reset delay*	Delay between the falling edge of the Data Ready output asynchronous Reset signal (DDRB) and the reset to digital zero transition of the Data Ready output signal (DR).
(TR)	*Rise time*	Time delay for the output DATA signals to rize from 20% to 80% of delta between low level and high level.
(TF)	*Fall time*	Time delay for the output DATA signals to fall from 80% to 20% of delta between low level and high level.
(PSRR)	*Power supply rejection ratio*	Ratio of input offset variation to a change in power supply voltage.
(NRZ)	*Non return to zero*	When the input signal is larger than the upper bound of the ADC input range, the output code is identical to the maximum code and the Out of Range bit is set to logic one. When the input signal is smaller than the lower bound of the ADC input range, the output code is identical to the minimum code, and the Out of range bit is set to logic one. (It is assumed that the input signal amplitude remains within the absolute maximum ratings).
(IMD)	*InterModulation Distortion*	The two tones intermodulation distortion (IMD) rejection is the ratio of either input tone to the worst third order intermodulation products. The input tones levels are at - 7dB Full Scale.
(NPR)	*Noise Power Ratio*	The NPR is measured to characterize the ADC performance in response to broad bandwidth signals. When using a notch-filtered broadband white-noise generator as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test.

7. APPLYING THE JTS8388B

7.1. TIMING INFORMATIONS

7.1.1. TIMING VALUE FOR JTS8388B

Timing values are given at chip inputs/outputs, taking into account pad and ESD protections capacitance, 2 mm (30 um diameter) bonding wire per pad, and specified termination loads.

Propagation delays in 50/75 ohms impedance traces are NOT taken into account for TOD and TDR.
Apply proper derating values corresponding to termination topology.

The min/max timing values are valid over the full temperature range in the following conditions :

Note 1 : Specified Termination Load (Differential output Datas and Data Ready) :

50 ohms resistor in parallel with 1 standard ECLinPS register from Motorola, (e.g : 10E452)
(Typical ECLinPS inputs shows a typical input capacitance of 1.5 pF (including package and ESD protections)
If addressing an output Dmux, take care if some Digital outputs do not have the same termination load and apply corresponding derating value given below.

Note 2 : Output Termination Load derating values for TOD and TDR :
~ 60 ps/pF or 75 ps per additional ECLinPS load.

Note 3 :Propagation time delay derating values have also to be applied for TOD and TDR :
~ 6 ps/mm (155 ps/inch) for TSEV8388B Evaluation Board.
Apply proper time delay derating value if a different dielectric layer is used.

7.1.2. PROPAGATION TIME CONSIDERATIONS

TOD and TDR Timing values are given from pin to pin and DO NOT include the additional propagation times between device pins and input/output termination loads. For the TSEV8388B Evaluation Board, the propagation time delay is 6ps/mm (155ps/inch) corresponding to 3.4 (@10GHz) dielectric constant of the RO4003 used for the Board.

If a different dielectric layer is used (for instance Teflon), please use appropriate propagation time values.

TD does NOT depend on propagation times because it is a differential data.
(TD is the time difference between Data Ready output delay and digital Data output delay)
TD is also the most straightforward data to measure, again because it is differential :
TD can be measured directly onto termination loads, with matched Oscilloscopes probes.

7.1.3. TOD - TDR VARIATION OVER TEMPERATURE

Values for TOD and TDR track each other over temperature (1 percent variation for TOD - TDR per 100 degrees Celsius temperature variation).

Therefore TOD - TDR variation over temperature is negligible. Moreover, the internal (onchip) and package skews between each Data TODs and TDR effect can be considered as negligible.

Consequently, minimum values for TOD and TDR are never more than 100 ps apart. The same is true for the TOD and TDR maximum values.

In other terms :
If TOD is at 950 ps, TDR will not be at 1420 ps (maximum time delay for TDR).
If TOD is at 1460 ps, TDR will not be at 910 ps (minimum time delay for TDR) However, external TOD - TDR values may be dictated by total digital datas skews between every TODs (each digital data) and TDR :
MCM Board , bonding wires and output lines lengths differences, and output termination impedance mismatches.

The external (on board) skew effect has NOT been taken into account for the specification of the minimum and maximum values for TOD-TDR.

7.1.4. PRINCIPLE OF OPERATION

The Analog input is sampled on the rising edge of external clock input (CLK,CLKB) after TA (aperture delay) of typically 250ps .
The digitized data is available after 4 clock periods latency (pipeline delay (TPD)), on clock rising edge, after 1160 ps typical propagation delay TOD.

The Data Ready differential output signal frequency (DR,DRB) is half the external clock frequency, that is it switches at the same rate as the digital outputs.

The Data Ready output signal (DR,DRB) switches on external clock falling edge after a propagation delay TDR of typically 1120 ps.

A Master Asynchronous Reset input command DRRB (ECL compatible single-ended input) is available for initializing the differential Data Ready output signal (DR,DRB) .This feature is mandatory in certain applications using interleaved ADCs or using a single ADC with demultiplexed outputs. Actually, without Data Ready signal initialization, it is impossible to store the output digital datas in a defined order.

7.2. PRINCIPLE OF DATA READY SIGNAL CONTROL BY DRRB INPUT COMMAND

7.2.1. DATA READY OUTPUT SIGNAL RESET

The Data Ready signal is reset on falling edge of DRRB input command, on ECL logical low level (-1.8V). DRRB may also be tied to VEE = - 5V for Data Ready output signal Master Reset. So long DRRB remains at logical low level, (or tied to VEE = - 5V), the Data Ready output remains at logical zero and is independant of the external free running encoding clock.

The Data Ready output signal (DR,DRB) is reset to logical zero after TRDR= 720 ps typical.

TRDR is measured between the -1.3V point of the falling edge of DRRB input command and the zero crossing point of the differential Data Ready output signal (DR,DRB).

The Data Ready Reset command may be a pulse of 1 ns minimum time width.

7.2.2. DATA READY OUTPUT SIGNAL RESTART

The Data Ready output signal restarts on DRRB command rising edge, ECL logical high levels (-0.8V).
DRRB may also be Grounded, or is allowed to float, for normal free running Data Ready output signal.

The Data Ready signal restart sequence depends on the logical level of the external encoding clock, at DRRB rising edge instant :

1) The DRRB rising edge occurs when external encoding clock input (CLK,CLKB) is LOW :
   The Data Ready output first rising edge occurs after half a clock period on the clock falling edge, after a delay time TDR = 1320 ps already defined hereabove.
2) The DRRB rising edge occurs when external encoding clock input (CLK,CLKB) is HIGH :
   The Data Ready output first rising edge occurs after one clock period on the clock falling edge, and a delay TDR = 1320ps.

Consequently, as the analog input is sampled on clock rising edge, the first digitized data corresponding to the first acquisition (N) after Data Ready signal restart (rising edge) is always strobed by the third rising edge of the data ready signal.
The time delay (TD1) is specified between the last point of a change in the differential output data (zero crossing point) to the rising or falling edge of the differential Data Ready signal (DR,DRB) (zero crossing point).

Note 1 : For normal initialization of Data Ready output signal, the external encoding clock signal frequency and level must be controlled.
It is reminded that the minimum encoding clock sampling rate for the ADC is 10 MSPS and consequently the clock cannot be stopped.

Note 2 : One single pin is used for both DRRB input command and die junction temperature monitoring.
Pin denomination will be DRRB/DIOD.(On former version denomination was DIOD.)
Temperature monitoring and Data Ready control by DRRB is not possible simultaneously.

7.3. ANALOG INPUTS (VIN) (VINB)

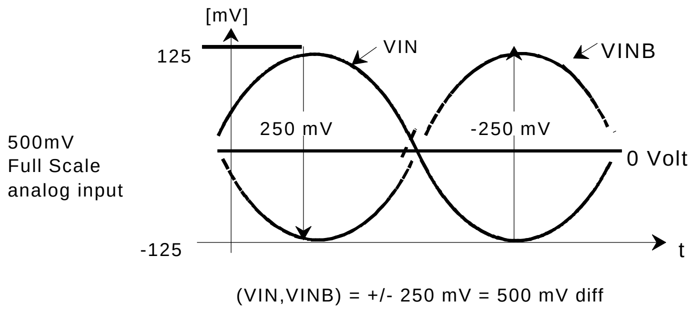
The analog input Full Scale range is 0.5 Volts peak to peak (Vpp), or -2 dBm into the 50 ohms termination resistor.

In differential mode input configuration, that means 0.25 Volt on each input, or +/- 125 mV around zero volt. The input common mode is GROUND.

The typical input capacitance is 0.4 pF in die form (JTS8388B), not taking into account the bond wires capacitance.

The input capacitance is mainly due to the pad capacitance, as the ESD protections are not connected (but present) on the inputs.

Differential inputs voltage span



Differential versus single ended analog input operation
The JTS8388B can operate at full speed in either differential or single ended configuration.
This is explained by the fact the ADC uses a high input impedance differential preamplifier stage, (preceeding the Sample and hold stage), which has been designed in order to be entered either in differential mode or single–ended mode.

This is true so long as the out of phase analog input pin VINB is 50 ohms terminated very closely to one of the neighboring shield ground pins (33? 35? 37) which constitute the local ground reference for the inphase analog input pin (VIN).

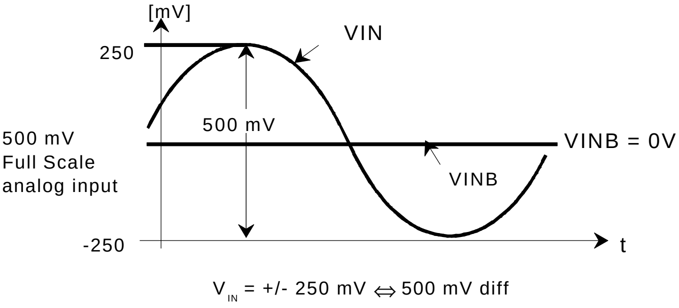
Thus the differential analog input preamplifier will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects.

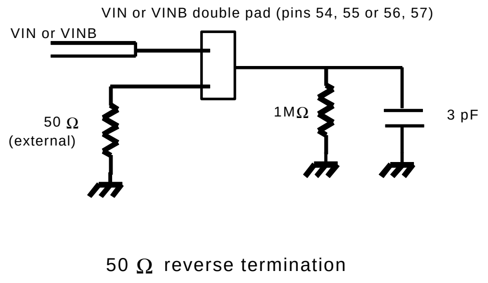
In typical single–ended configuration, enter on the (VIN) input pin, with the inverted phase input pin (VINB) grounded through the 50 ohms termination resistor.

In single–ended input configuration, the in-phase input amplitude is 0.5 Volt peak to peak,centered on 0V. (or -2 dBm into 50 ohms.)
The inverted phase input is at ground potential through the 50 ohms termination resistor.

However, dynamic performances can be somewhat improved by entering either analog or clock inputs in differential mode.

Typical Single ended analog input configuration





7.4. CLOCK INPUTS (CLK) (CLKB)

The JTS8388B can be clocked at full speed without noticeable performance degradation in either differential or single ended configuration.
This is explained by the fact the ADC uses a differential preamplifier stage for the clock buffer, which has been designed in order to be entered either in differential or single–ended mode.

7.4.1. SINGLE ENDED CLOCK INPUT (GROUND COMMON MODE)

Although the clock inputs were intended to be driven differentially with nominal -0.8V / -1.8V ECL levels, the JTS8388B clock buffer can manage a single–ended sinewave clock signal centered around 0 Volt. This is the most convenient clock input configuration as it does not require the use of a power splitter.

No performance degradation (e.g. : due to timing jitter) is observed in this particular single–ended configuration up to 1.2GSPS Nyquist conditions (Fin = 600 MHz).

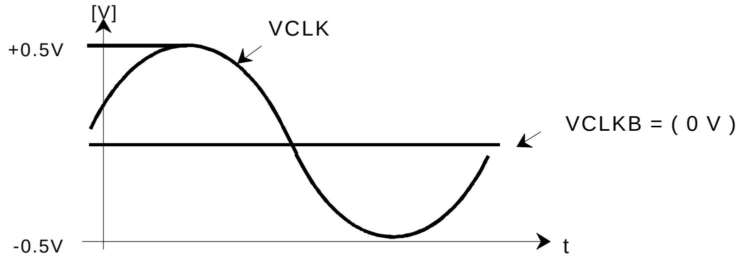
This is true so long as the inverted phase clock input pin is 50 ohms terminated very closely to one of the neighbouring shield ground pin, which constitutes the local Ground reference for the inphase clock input.

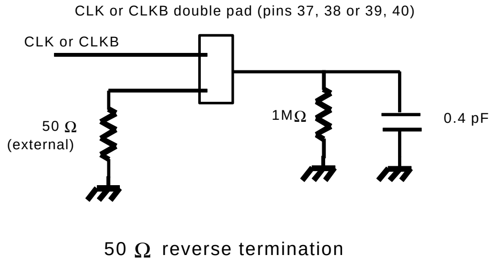
Thus the JTS8388B differential clock input buffer will fully reject the local ground noise (and any capacitively and inductively coupled noise) as common mode effects.
Moreover, a very low phase noise sinewave generator must be used for enhanced jitter performance.

The typical inphase clock input amplitude is 1 Volt peak to peak, centered on 0 Volt (ground) common mode.
This corresponds to a typical clock input power level of 4 dBm into the 50 ohms termination resistor.
Do not exceed 10 dBm to avoid saturation of the preamplifier input transistors.
The inverted phase clock input is grounded through the 50 ohms termination resistor.

Single ended Clock input (Ground common mode)

VCLK common mode = 0 Volt
VCLKB=0 Volt
4 dBm typical clock input power level
(into 50 ohms termination resistor)





Note 1 : Do not exceed 10 dBm into the 50 ohms termination resistor for single clock input power level.

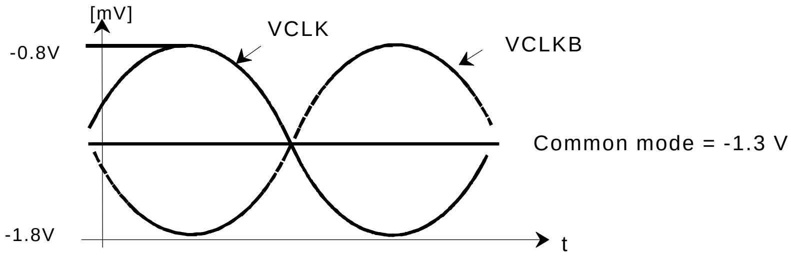
7.4.2. DIFFERENTIAL ECL CLOCK INPUT

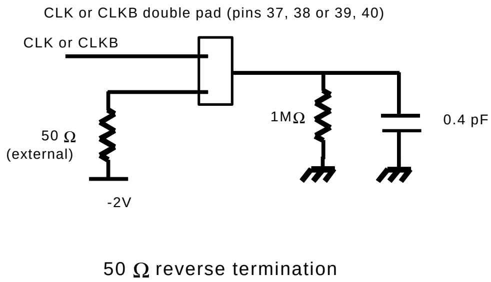
The clock inputs can be driven differentially with nominal -0.8V / -1.8V ECL levels.

In this mode, a low phase noise sinewave generator can be used to drive the clock inputs, followed by a power splitter (hybrid junction) in order to obtain 180 degrees out of phase sinewave signals. Biasing tees can be used for offseting the common mode voltage to ECL levels.

Note : As the biasing tees propagation times are not matching, a tunable delay line is required in order to ensure the signals to be 180 degrees out of phase especially at fast clock rates in the GSPS range.

Differential Clock inputs (ECL Levels)

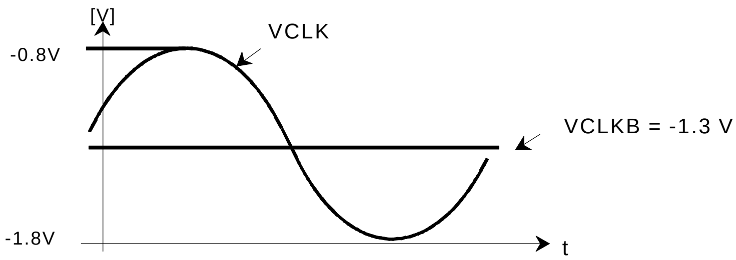




7.4.3. SINGLE ENDED ECL CLOCK INPUT

In single–ended configuration enter on CLK (resp. CLKB) pin , with the inverted phase Clock input pin CLKB (respectively CLK) connected to -1.3V through the 50 ohms termination resistor.
The inphase input amplitude is 1 Volt peak to peak, centered on -1.3 Volt common mode.

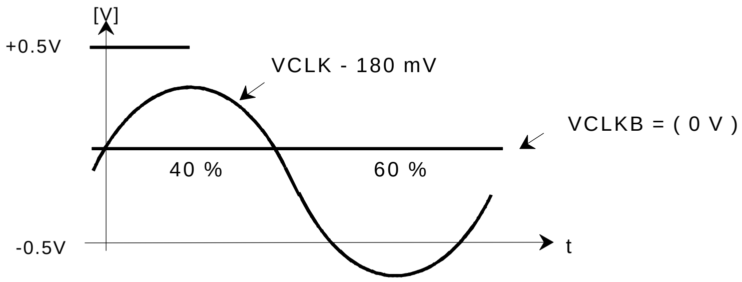
Single ended Clock input (ECL):
VCLK common mode = -1.3 Volt.
VCLKB = -1.3 Volt



7.5. CLOCK SIGNAL DUTY CYCLE ADJUST

At fast sampling rates, (1 Gsps and above), the device performance (especially the SNR) may be improved by tuning the Clock duty cycle (CLK,CLKB).
In single ended configuration, when using a sinewave clock generator, the clock signal duty cycle can be easily adjusted by simply offseting the inphase clock signal using a biasing tee, (as the out of phase clock input is at ground level).

Single ended Clock input (Inphase clock input common mode shifted)
VCLK common mode = -180mV
VCLKB = 0 Volt



Note 1 : Do not exceed 10 dBm into the 50 ohms termination resistor for single clock input power level.
Note 2 : For an input CLK signal of 4 dBm into 50 ohms, the typical offset value to achieve a 40 / 60 clock duty cycle is -180 mV on CLK.

7.6. NOISE IMMUNITY INFORMATIONS

Circuit noise immunity performance begins at design level.
Efforts have been made on the design in order to make the device as insensitive as possible to chip environment perturbations resulting from the circuit itself or induced by external circuitry.
(Cascode stages isolation, internal damping resistors, clamps, internal (onchip) decoupling capacitors.)

Furthermore, the fully differential operation from analog input up to the digital outputs provides enhanced noise immunity by common mode noise rejection.
Common mode noise voltage induced on the differential analog and clock inputs will be canceled out by these balanced differential amplifiers.

Moreover, proper active signals shielding has been provided on the chip to reduce the amount of coupled noise on the active inputs :
The analog inputs and clock inputs of the TS8388B device have been surrounded by ground pins, which must be directly connected to the external ground plane.

7.7. DIGITAL OUTPUTS

The JTS8388B differential output buffers are internally 75 ohms loaded. The 75 ohms resistors are connected to the digital ground pins through a -0.8v level shift diode (see Figures 3,4,5 on next page).

The JTS8388B output buffers are designed for driving 75 ohms (default) or 50 ohms properly terminated impedance lines or coaxial cables.
An 11 mA bias current flowing alternately into one of the 75 ohms resistors when switching ensures a 0.825 V voltage drop across the resistor (unterminated outputs).
The VPLUSD positive supply voltage allows the adjustment of the output common mode level from -1.2V (VPLUSD=0V for ECL output compatibility) to +1.2V (VPLUSD=2.4V for LVDS output compatibility).
Therefore,the single ended output voltages vary approximately between -0.8V and -1.625V, (outputs unterminated), around
-1.2V common mode voltage.

Three possible line driving and back-termination scenarios are proposed (assuming VPLUSD=0V) :

1) 75 Ohms impedance transmission lines, 75 ohms differentialy terminated (Fig. 3) :
Each output voltage varies between -1V and -1.42V (respectively +1.4V and +1V), leading to +/- 0.41V =0.825 V in differential, around -1.21 V (respectively +1.21V) common mode for VPLUSD=0V (respectively 2.4V).

2) 50 ohms impedance transmission lines, 50 ohms differentialy termination (Fig. 4) :
Each output voltage varies between -1.02V and -1.35V (respectively +1.38V and +1.05V), leading to +/- 0.33V=660 mV in differential, around -1.18V (respectively +1.21V) common mode for VPLUSD=0V (respevtively 2.4V).

3) 75 ohms impedance open transmission lines (Fig. 5) :
Each output voltage varies between -1.6 V and -0.8 V (respectively +0.8V and +1.6V), which are true ECL levels, leading to +/- 0.8V=1.6V in differential, around -1.2V (respectively +1.2V) common mode for VPLUSD=0V (respectively 2.4V).
Therefore, it is possible to drive directly high input impedance storing registers, without terminating the 75 ohms transmission lines.
In time domain, that means that the incident wave will reflect at the 75 ohms transmission line output and travel back to the generator (i.e. the 75 ohms data output buffer). As the buffer output impedance is 75 ohms, no back reflection will occur.

Note : This is no longer true if a 50 ohms transmission line is used, as the latter is not matching the buffer 75 ohms output impedance.

Each differential output termination length must be kept identical .
It is recommended to decouple the midpoint of the differential termination with a 10 nF capacitor to avoid common mode perturbation in case of slight mismatch in the differential output line lengths.

Too large mismatches (keep < a few mm) in the differential line lengths will lead to switching currents flowing into the decoupling capacitor leading to switching ground noise.

The differential output voltage levels (75 or 50 ohms termination) are not ECL standard voltage levels, however it is possible to drive standard logic ECL circuitry like the ECLinPS logic line from MOTOROLA.

At sampling rates exceeding 1GSPS, it may be difficult to trigger the HP16500 or any other Acquisition System with digital outputs.
It becomes necessary to regenerate digital data and Data Ready by means of external amplifiers, in order to be able to test the JTS8388B at its optimum performance conditions.

7.7.1. DIFFERENTIAL OUTPUT LOADING CONFIGURATIONS (LEVELS FOR ECL COMPATIBILITY)

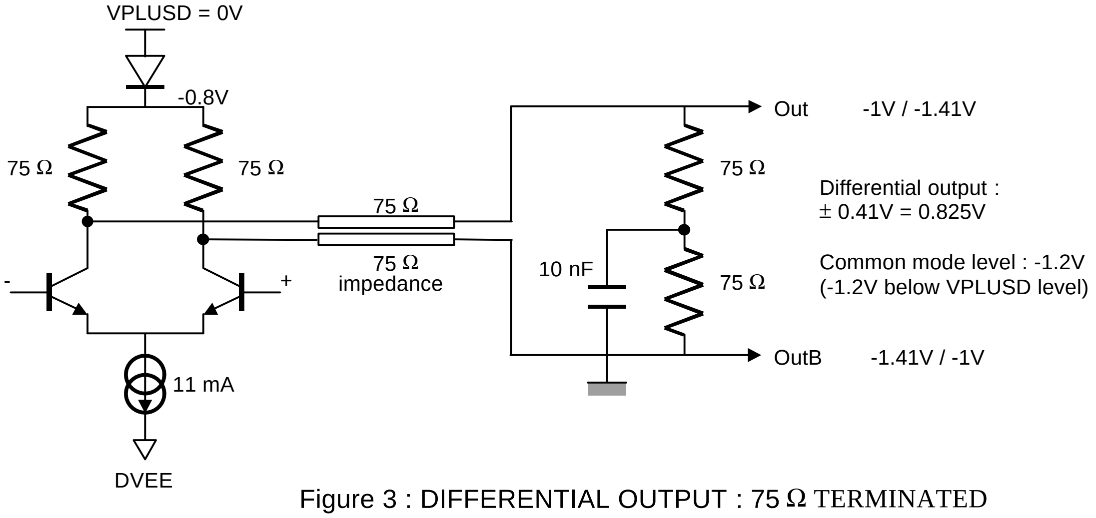


Figure 3 : DIFFERENTIAL OUTPUT : 75 Ω TERMINATED

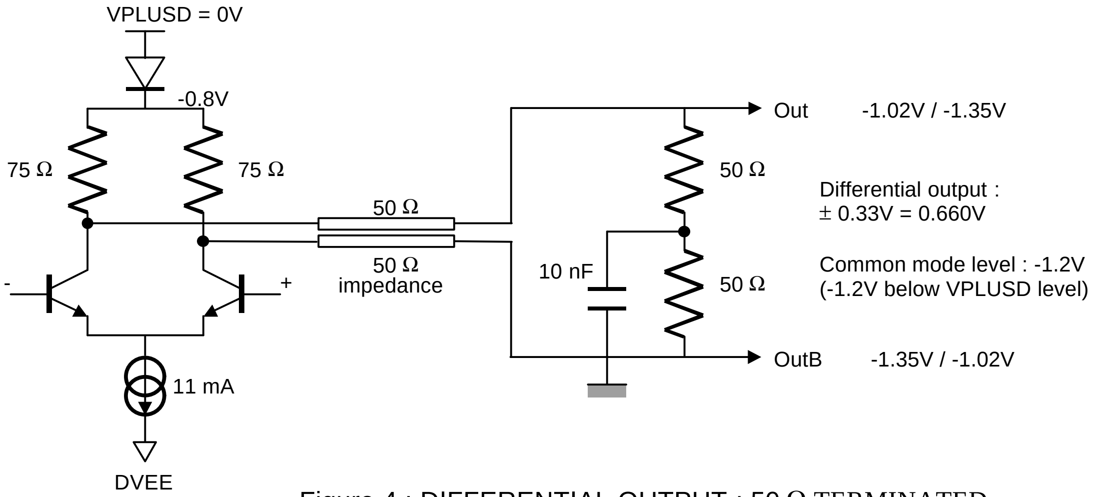


Figure 4 : DIFFERENTIAL OUTPUT : 50 Ω TERMINATED

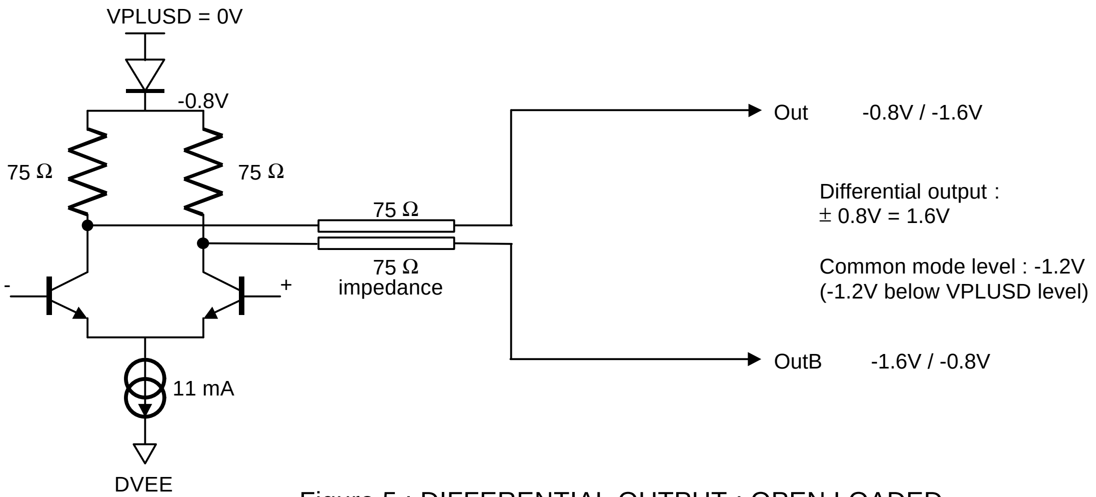


Figure 5 : DIFFERENTIAL OUTPUT : OPEN LOADED

7.7.2. DIFFERENTIAL OUTPUT LOADING CONFIGURATIONS (LEVELS FOR LVDS COMPATIBILITY)

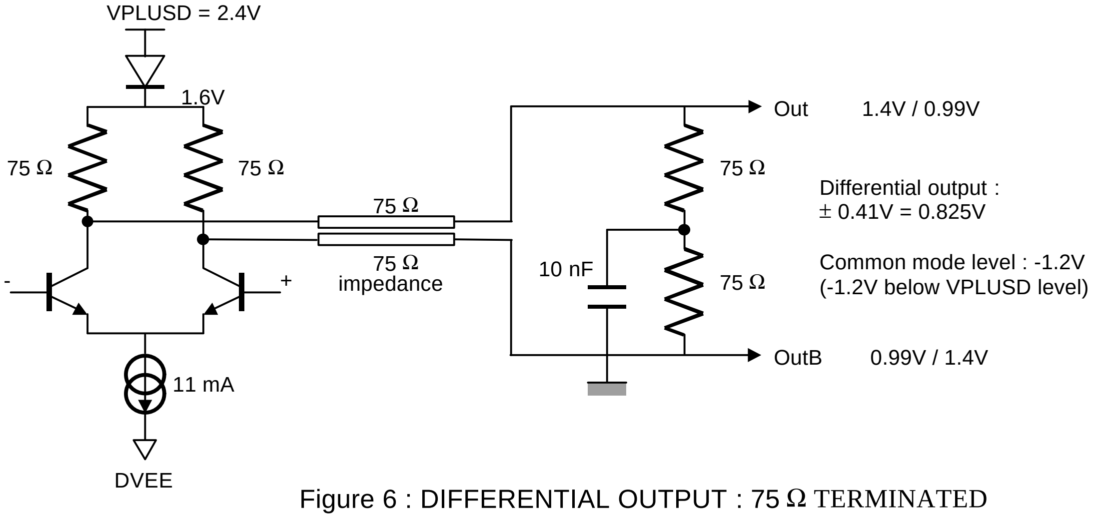


Figure 6 : DIFFERENTIAL OUTPUT : 75 Ω TERMINATED

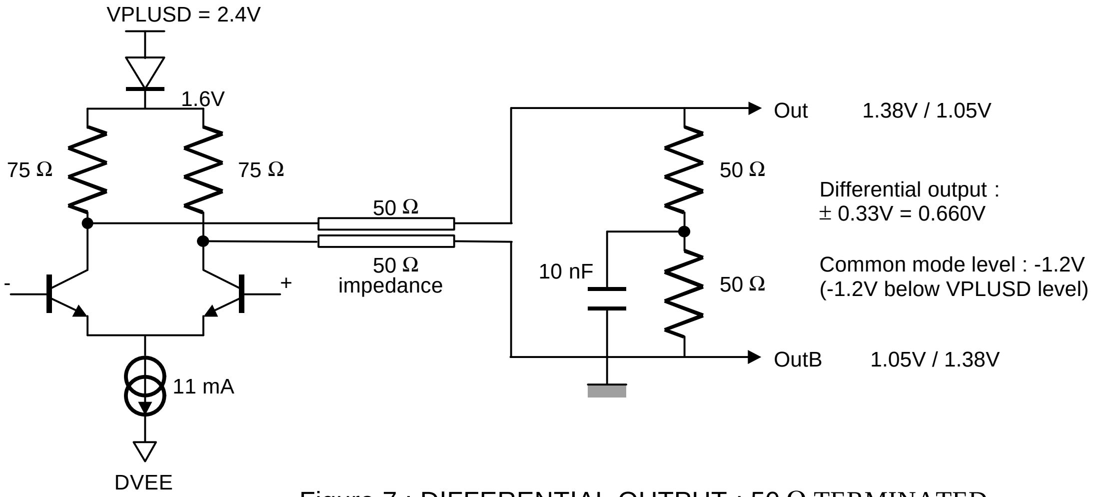


Figure 7 : DIFFERENTIAL OUTPUT : 50 Ω TERMINATED

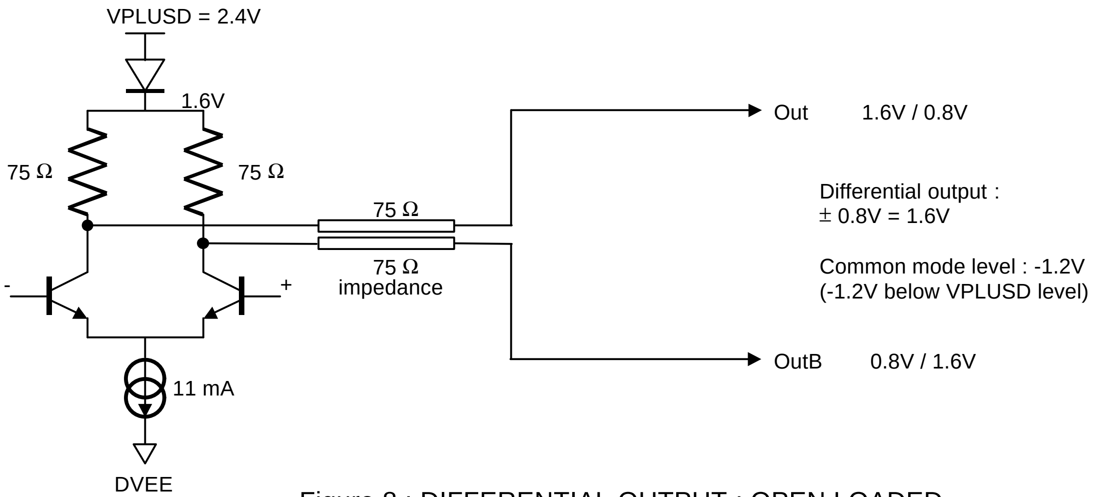


Figure 8 : DIFFERENTIAL OUTPUT : OPEN LOADED

7.8. OUT OF RANGE BIT

An Out of Range (OR,ORB) bit is provided that goes to logical high state when the input exceeds the positive full scale or falls below the negative full scale.
When the analog input exceeds the positive full scale, the digital output datas remain at high logical state, with (OR,ORB) at logical one.
When the analog input falls below the negative full scale, the digital outputs remain at logical low state, with (OR,ORB) at logical one again.

7.9. GRAY OR BINARY OUTPUT DATA FORMAT SELECT

The JTS8388B internal regeneration latches indecision (for inputs very close to latches threshold) may produce errors in the logic encoding circuitry and leading to large amplitude output errors.

This is due to the fact that the latches are regenerating the internal analog residues into logical states with a finite voltage gain value (Av) within a given positive amount of time $\Delta(t)$:
Av= $\exp(\Delta(t)/\tau)$, with τ the positive feedback regeneration time constant.

The JTS8388B has been designed for reducing the probability of occurence of such errors to approximately 10^{-13} (targetted for the JTS8388B at 1GSPS).

A standard technique for reducing the amplitude of such errors down to +/-1 LSB consists to output the digital datas in Gray code format.
Though the JTS8388B has been designed for featuring a Bit Error Rate of 10^{-13} with a binary output format, it is possible for the user to select between the Binary or Gray output data format, in order to reduce the amplitude of such errors when occuring, by storing Gray output codes.

Digital Datas format selection :
BINARY output format if GORB is floating or VCC.
GRAY output format if GORB is connected to ground (0V).

7.10. TS8388 B THERMAL REQUIREMENTS

The JTS8388B is currently mounted on its dedicated Chip Evaluation Board (CEB), with fulfills the device thermal requirements in still air at room temperature.

For operation in the military temperature range, forced convection is required to maintain the device junction temperature below the specified maximum value.

The JTS8388B power dissipation is 3.6 Watt at 70°C junction temperature, and 3.8 Watt at 125°C junction temperature. The die dimensions are 2.44 mm x 3 mm = 7.32 mm².

The maximum junction temperature is 145°C.

To manage correctly the power dissipation of the JTS8388B device, the following thermal fixture profile is used, taking into account the die dimensions and power dissipation :
7.5 C°/W typical value for die attach Ag filled Epoxy glue, but depending on gllue film thickness.
0.5 C°/W Copper block.
1 C°/W isolation foil.
6.5 C°/W heatsink (still air).

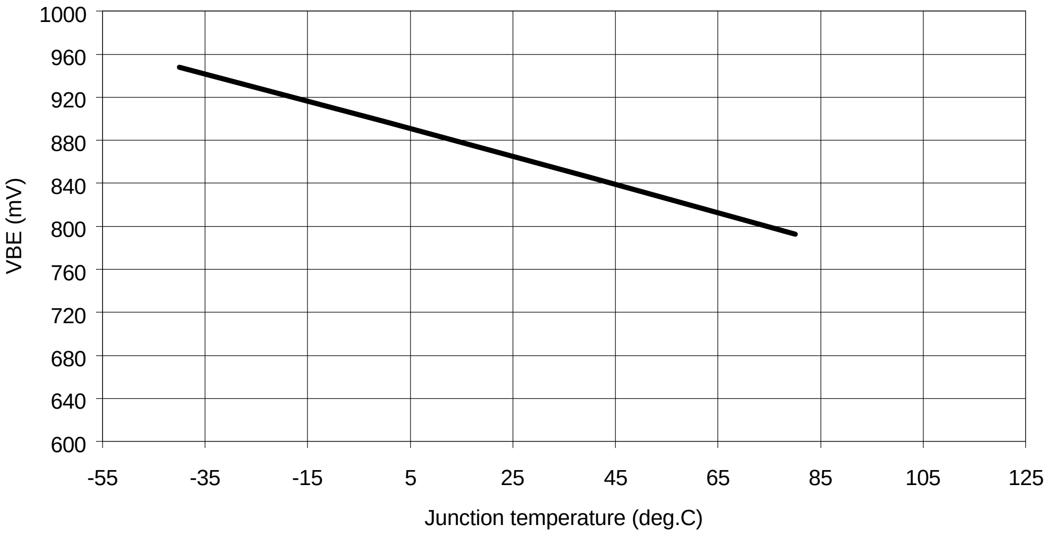
The heatsink used is the 3334B pin fin heatsink from Thermalloy, (also used cooling the 604 Power PC µP). Its dimensions are 50.70 mm x 50.39 mm = (1.996 inch x 1.984 inch x 0.650 inch).

The measured die junction to ambient thermal resistance (RTHJA) for the Chip Evaluation Board is approximately 15.5 C/W in still air.

At room temperature (25°C), this yields to a device junction temperature of approximately 80°C, in thermal steady state conditions.

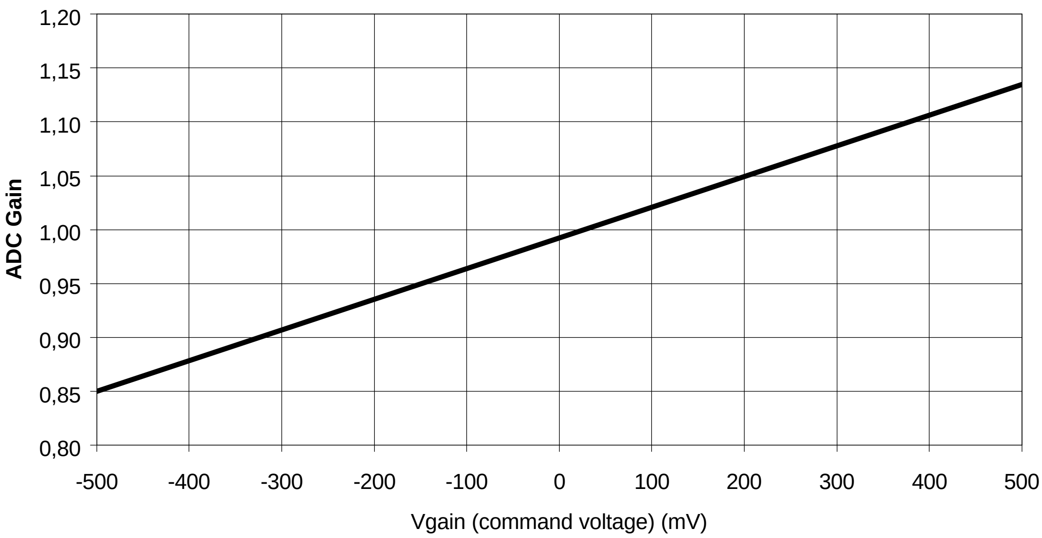
7.11. DIODE PAD 32

The DIODE pad 32 is provided for die junction temperature monitoring.
The operating die junction temperature must be kept below145°C, therefore an adequate cooling system has to be set up.
The diode mounted transistor measured Vbe value versus junction temperature is given below.



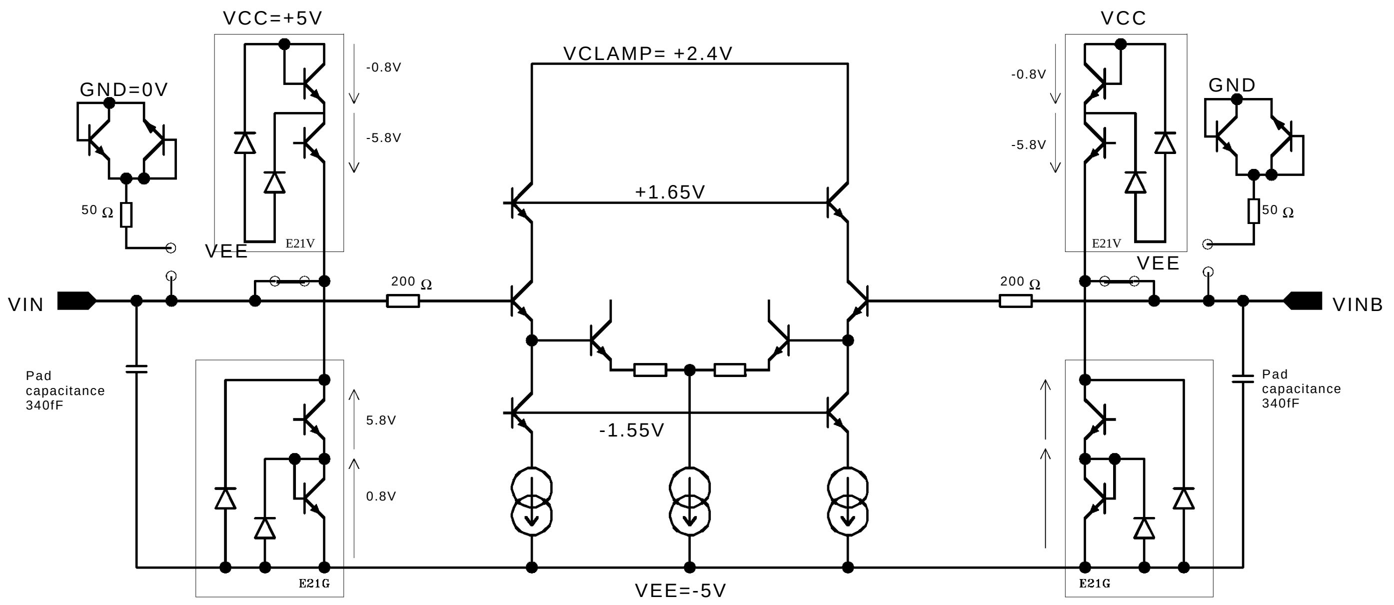
7.12. ADC GAIN CONTROL PAD 38

The ADC gain is adjustable by the means of the PAD 38 (input impedance is 1MΩ in parallel with 2pF)
The gain adjust transfer function is given below :



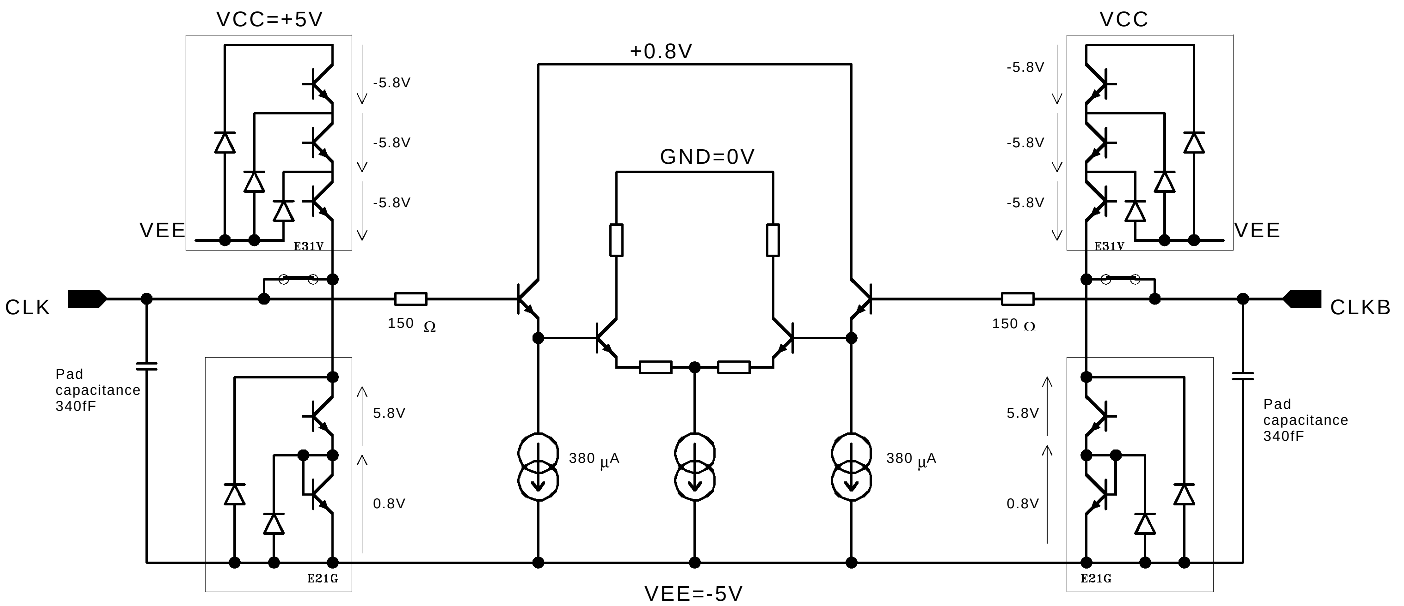
8. EQUIVALENT INPUT / OUTPUT SCHEMATICS

8.1. EQUIVALENT ANALOG INPUT CIRCUIT AND ESD PROTECTIONS



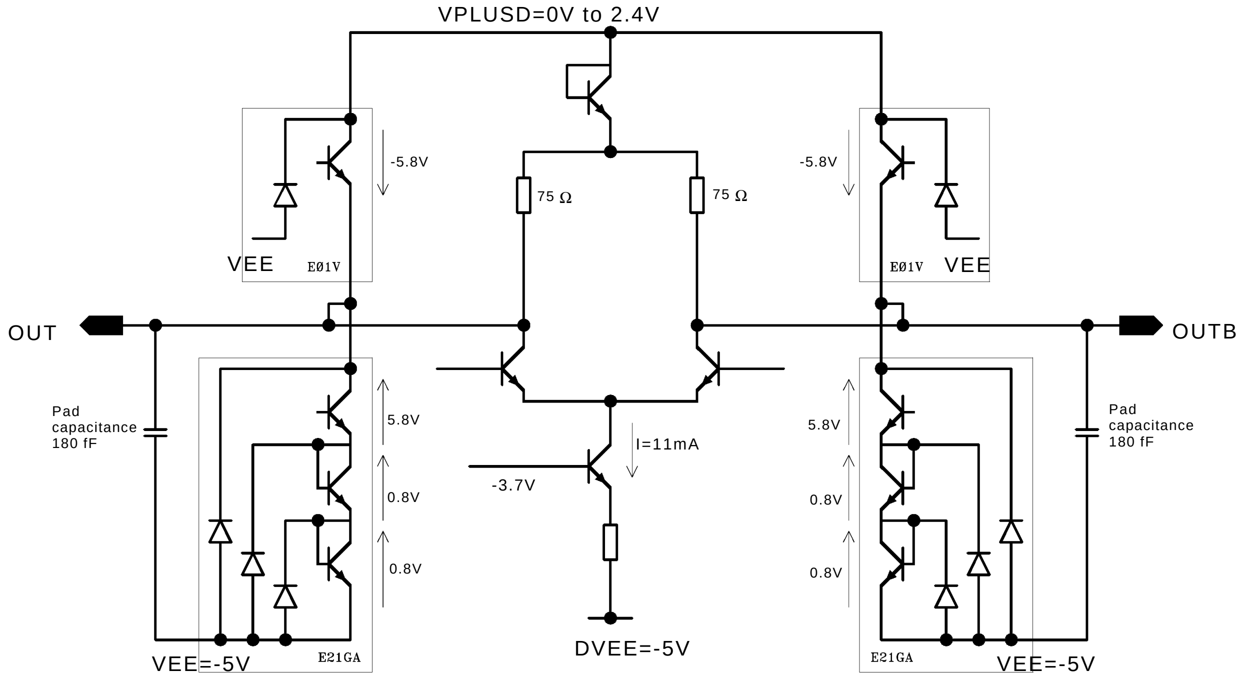
Note : the ESD protections are present but not connected for Vin and Vinb

8.2. EQUIVALENT ANALOG CLOCK INPUT CIRCUIT AND ESD PROTECTIONS



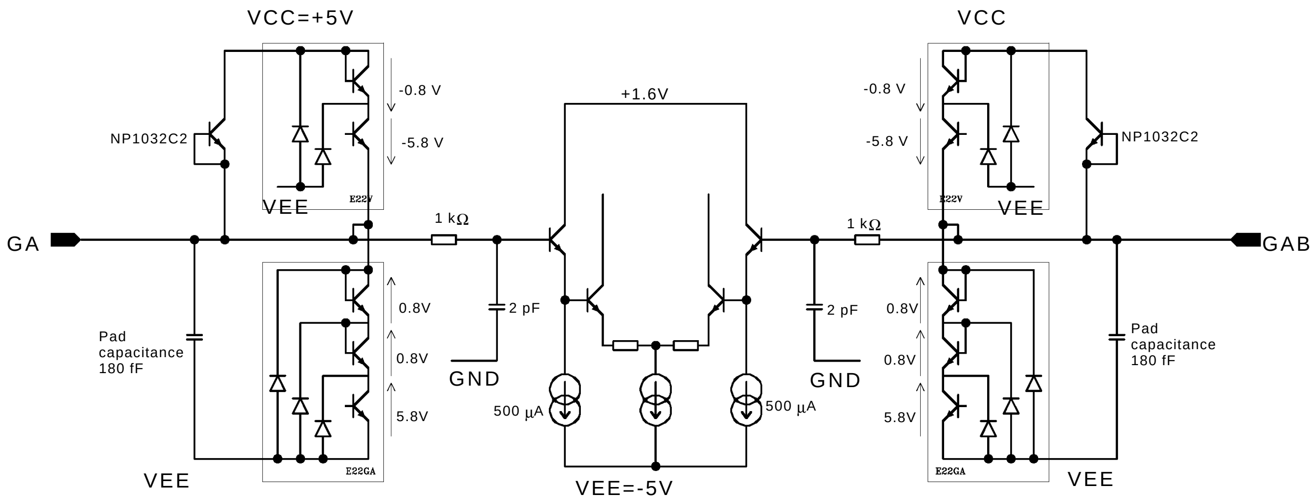
Note : the ESD protections are present but not connected for Clk and Clkb

8.3. EQUIVALENT DATA OUTPUT BUFFER CIRCUIT AND ESD PROTECTIONS



Note : the ESD protection equivalent capacitance is 150 fF.

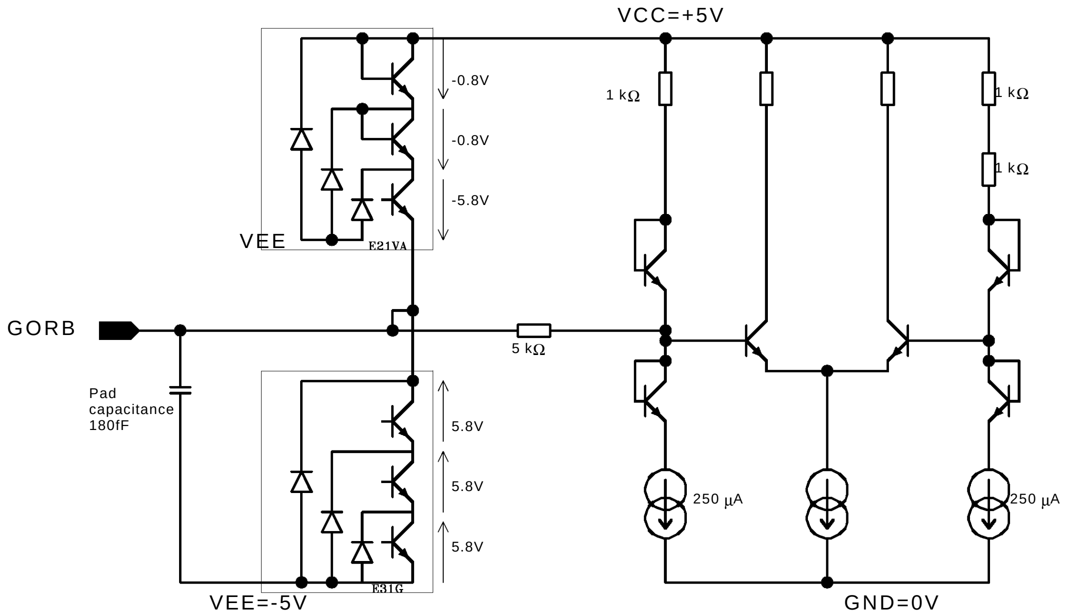
8.4. ADC GAIN ADJUST EQUIVALENT INPUT CIRCUITS AND ESD PROTECTIONS



Note : the ESD protection equivalent capacitance is 150 fF.

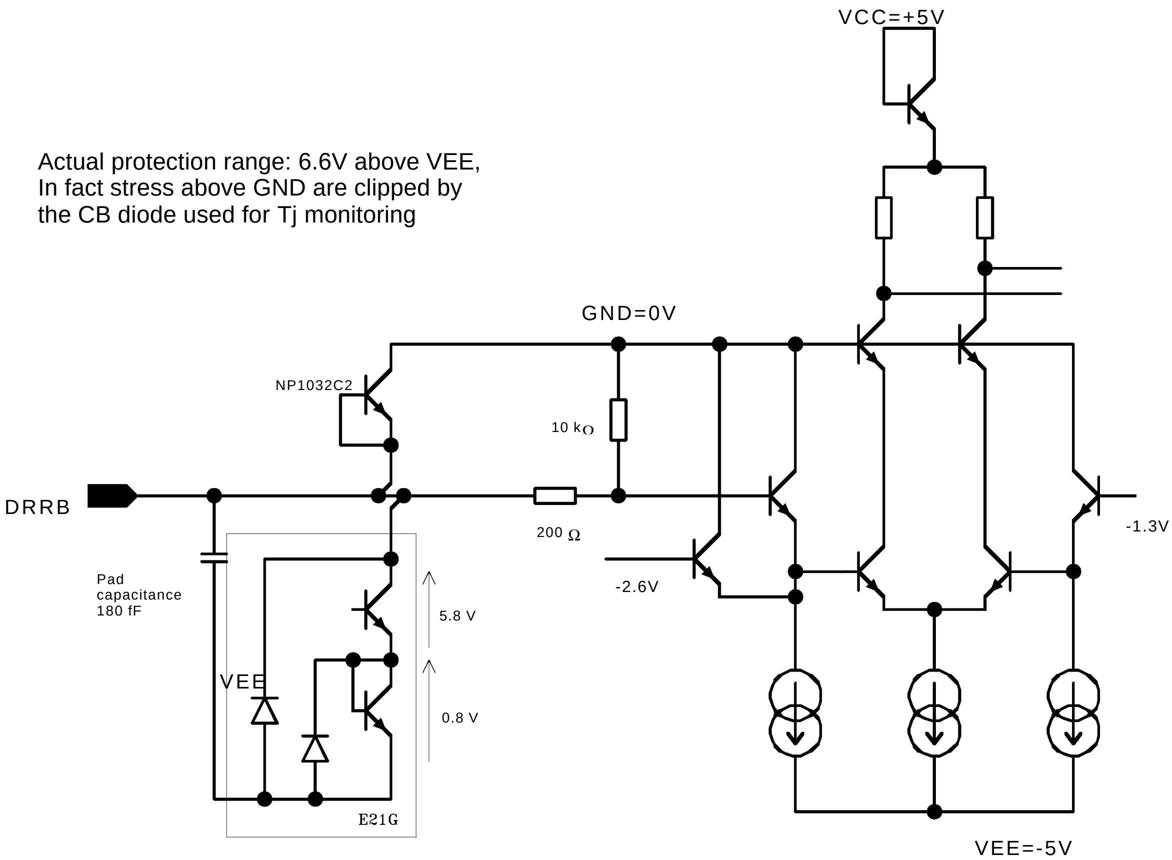
8.5. GORB EQUIVALENT INPUT SCHEMATIC AND ESD PROTECTIONS

GORB: gray or binary select input; floating or tied to VCC -> binary



Note : the ESD protection equivalent capacitance is 150 fF.

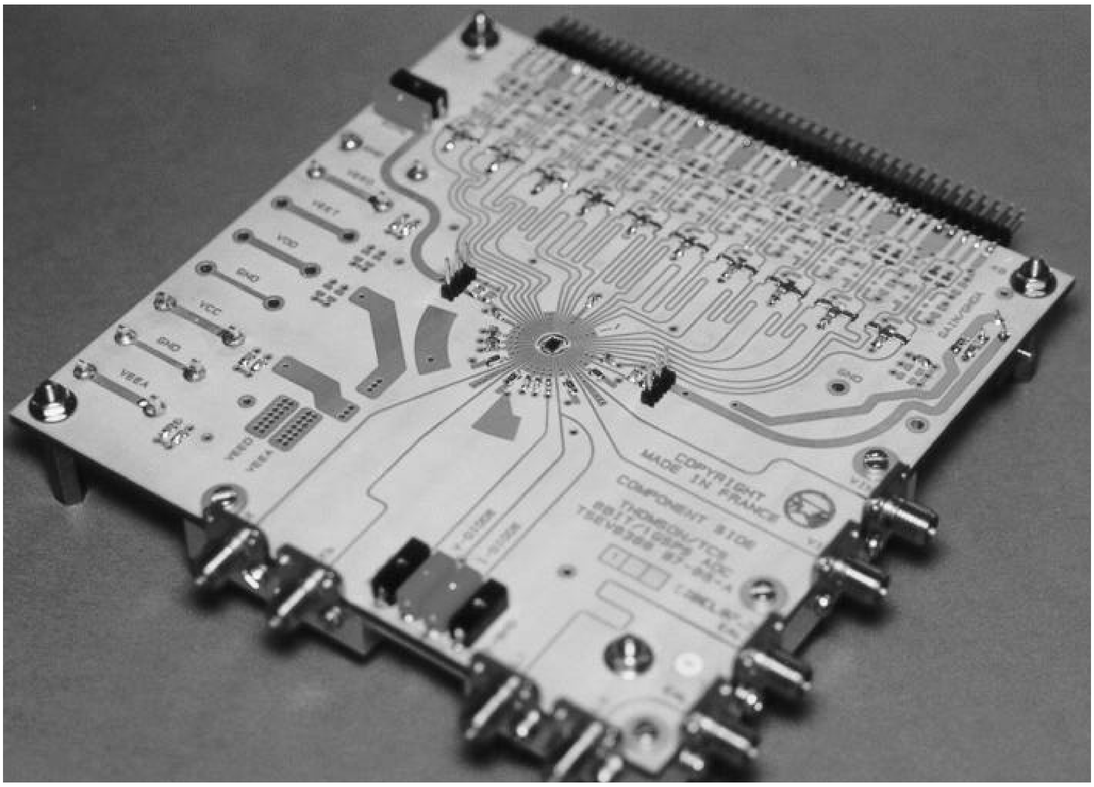
8.6. DRRB EQUIVALENT INPUT SCHEMATIC AND ESD PROTECTIONS



Note : the ESD protection equivalent capacitance is 150 fF.

9. TSEV8388B : DEVICE EVALUATION BOARD

For complete specification, see separate TSEV8388B document.



GENERAL DESCRIPTION

The TSEV8388B Evaluation Board (CEB) is a prototype board which has been designed in order to facilitate the evaluation and the characterization of the JTS8388B device up to its 2 GHz full power bandwidth at up to 1 Gsps in the military temperature range.

The high speed of the JTS8388B requires careful attention to circuit design and layout to achieve optimal performance.

This four metal layer board with internal ground plane has the adequate functions in order to allow a quick and simple evaluation of the JTS8388B ADC performances over the temperature range.

The TSEV8388B Evaluation Board is very straightforward as it only implements the JTS8388B ADC, SMA connectors for input / output accesses and a 2.54 mm pitch connector compatible with HP16500C high frequency probes.

The board also implements a de–embedding fixture in order to facilitate the evaluation of the high frequency insertion loss of the input microstrip lines, and a die junction temperature measurement setting.

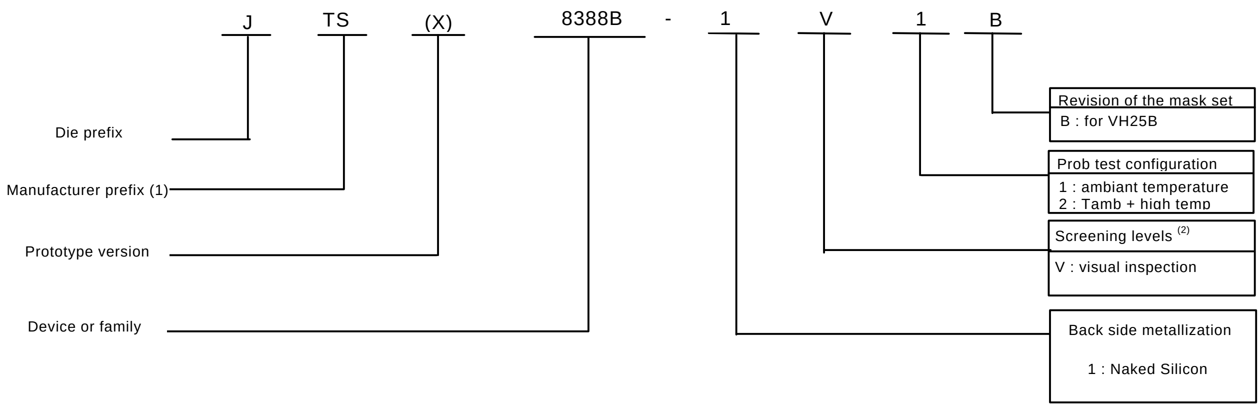
The board is constituted by a sandwich of two dielectric layers, featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain and extended temperature range.

The board dimensions are 130 mm x 130 mm.

The board set comes fully assembled and tested, with the JTS8388B die installed.

10. ORDERING INFORMATION

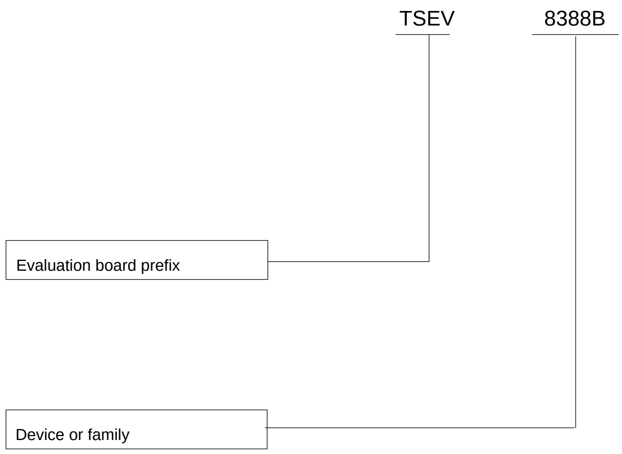
Die form



(1) ATMEL-GRENOBLE

(2) For availability of the different versions, contact your ATMEL-Grenoble sales office

Evaluation board



APPENDIX

DATASHEET STATUS		VALIDITY
Objective specification	This datasheet contains target and goal specification for discussion with customer and application validation.	Before design phase.
Target specification	This datasheet contains target and goal specification for product development.	Valid during the design phase.
Preliminary specification Alpha-site	This datasheet contains preliminary data. Additional data may be published later ; could include simulation results.	Valid before the characterization phase.
Preliminary specification Beta-site	This datasheet contains also characterization results.	Valid before the industrialization phase.
Product specification	This datasheet contains final product specifiaction.	Valid for production purpose.
Limiting values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		

LIFE SUPPORT APPLICATIONS

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